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Maxim integrated’s ceo, Tunc Doluca takes a few questions from EE Times Europe on analog, MEMS and the company’s strategy for the future.

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WHITEPAPERS
The future of video surveillance is hyperspectral

By Julien Happich

FREEZE! YOU’RE BLUSHING, we see your blood pumping abnormally fast and our analytical software tells us that you contravene crowd flow statistics, which is yet another reason to closely inspect and match your 3D facial features to our would-be criminal database, that is, anyone we have on record for citizenship.

Privacy advocate groups may manage to mute two-way audio surveillance cameras in some countries and the level of video coercion may not be felt so strongly by passers-by as most people are unaware of the level of analytics and geo-fencing that newly installed IP-connected HD surveillance cameras bring with them. But new surveillance cameras are no longer installed in a “record just-in-case then delete” scheme, in fact they are already adding their bulk of big data to the cloud.

With Imec’s recent announcement that it now supplies hyperspectral imaging sensor technology to strategic partners for its deployment into commercial camera solutions including for global security markets, you can be sure this new capability will blend-in with the latest surveillance trends such as HD resolution and to some extent, stereoscopic vision.

Of course, hyperspectral imaging is amazingly efficient at discriminating materials for sorting products, at identifying substances to check the freshness of foodstuff or to detect hazardous or illicit ones in airports. Implementing this technology into industrial machine vision or medical imaging can bring huge benefits to society. Medical applications are plentiful, from skin and tissue analysis for cancer detection to blood vessel imaging, or bacteria detection based on characteristic spectra.

Because until now they were quite costly and bulky, hyperspectral imaging systems were mostly used in high-end remote sensing instruments such as satellites and airborne systems (for precision agriculture to assess crop quality or to identify different types of lands, contamination etc.). But imec’s breakthrough using narrow-band spectral filters at pixel level, applied through semiconductor thin-film processing, means that compact hyperspectral image sensors could be mass produced at low cost. This is a boon for camera vendors as it opens up new markets.

Yet, where will this drive surveillance? How about performing real-time video analytics on your health status, churning data out of your skin’s spectral signature and combining this with crowd control tactics or even discriminating video geofencing? How about food and beverage vending machines spotting your blood-sugar level and making decisions (delivering a service or reversing to an “out of order” status) or reporting to insurance companies based on unstated health policies?

Not anything you would notice from looking back at that seemingly innocuous lens.

How much surveillance data is enough?
The answer by authoritarian regimes is definitely “as much as technologically feasible”. It does not differ much from what large commercial companies would want when scrutinizing their customers, except sometimes they get blamed for their lack of transparency. And since it’s “for your own good”, why would you blame your government for being even more hungry for such data?

The worldwide market for video surveillance equipment is expected to expand by more than 12 percent this year, according to market research firm IHS Technology, and any new feature that can help manufacturers differentiate from competition is good enough.

Among Imec’s key partners for developing this technology is Adimec from The Netherlands, who offers to customize its cameras for defense & security imaging applications. Featuring a full HD (1920x1080 pixels at 30 or 60 frames per second) electro-optical sensor module, the company’s TMX-DHD series increases detection, recognition and identification capabilities, according to what is on their website.

Another partner, 3D-One (The Netherlands) offers to couple high-resolution imaging and spectroscopy in its MO-50 and MO-60 series camera modules, combined with analysis and visualization software to extract the spectral information. The same company provides 3D (stereoscopic) HD imaging modules and analytical solutions to “accurately track people in a busy scene, such as a hall terminal or shopping mall” as it advertises on its website. Surely time will come when all these capabilities will be merged as a selling argument.

Italian partner Tattile specializes in programming and developing Automatic Numberplate Recognition (ANPR) solutions, it offers mainly products for tolling, speed enforcement, traffic tracking and access control. Again, integrating hyperspectral imaging to its on-board embedded analytic solutions is probably on the agenda.

Now the last partner cited is BaySpec (USA), who brought to market the OCI-1000, claimed to be the world’s first handheld hyperspectral imager. The palm-sized ‘point-and-shoot’ device is able to acquire full, continuous visible and near infrared hyperspectral data.
Innovator in Signal Capture & Recreate

In 1939, Anritsu developed the AC-bias magnetic sound recorder – a key part of the tape recorder. In 2007, Anritsu marked another first with its launch of a one-box spectrum analyzer and signal generator which also provided a unique capture and recreate function. Today, Anritsu’s MS2690A and MS2830A spectrum/signal analyzer series provides an all-in-one solution that captures data and signals in the field and recreates them seamlessly in the lab, maximizing product quality and efficiency.

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Europe’s ‘Airbus of chips’ taxis to take-off position

By Christoph Hammerschmidt

Almost two years after EC commissioner Neelie Kroes aired the idea of creating a pan-European industry initiative to transplant the continent’s success in aircraft building to the semiconductor business, the industry gets moving. At the SEMI Industry Strategy Symposium (ISS Europe) in February in Salzburg, semiconductor bigwigs set the course.

A few days ahead of the meeting in Salzburg, the European Commission published a roadmap which defined technology areas in which Europe’s industry is strong enough to let Kroes’ high-flying goals appear realistic. The EC Commissioner for the Digital Agenda aims high: within the next ten years, the European economy can double the value of chips produced here, she believes. In other emerging markets, for example in the Internet of Things, European companies should be able to grab 60 percent of the worldwide business by 2020. And in technology segments where Europe lost its past glory like mobile and wireless communications, the EC hopes that European companies reinvigorate and capture 20 percent of the projected future growth.

These are the goals. The roadmap details the industry segments where Europe can realistically entertain hopes for a global leading position, and defines which action to take in order to win or defend such a top position. These segments are automotive, energy, industrial automation, security and intellectual property as well as semiconductor materials and equipment. At the same time, the paper defines future growth areas where the European semiconductor industry should stake its claims: besides the Internet of Things, these growth areas include what the experts call Smart-X markets - with X standing for things like homes, grids and similar notions.

All these figures and definitions result from consultations within the Electronics Leaders Group (ELG) which Neelie Kroes brought into being about a year ago. The ELT comprises eleven top executives from major European chip making companies, equipment manufacturers and research organisations.

At the ISS in Salzburg it was apparent that the roadmap provides a common ground for the European industry for future action - no one of the participants seriously questioned the paper. Nevertheless a panel discussion at the meeting with industry pundits - and some of them also were ELG members - showed that there is still a significant need to clarify the details of the way ahead. “Europe clearly recognizes that micro and nano electronics is a key enabler for many of the technologies in which it wants to be a top player”, said Infineon CEO Reinhard Ploss. “To achieve the goals described we do not only have to focus on chip manufacturing - it is also a matter of differentiating in end markets and competence. It seems clear to me that we also have to create new markets for our chips.” He added that the first priority is to develop outstanding technology - then the production can be retained in Europe, not the other way around.

Ruther Wijburg, CEO of Globalfoundries Dresden and like Ploss an ELG member pointed out that Europe already has a “brilliant platform” to start from, referring to the existing manufacturing base. Wijburg however pointed out that the need of Europe and the need of a company that has to act globally is not necessarily 100 percent identical. “A company like us always has to make its decisions on a global basis.”

He nevertheless agreed that in automotive and other market segments like medical electronics there are enormous business chances in Europe. In order to achieve the goals defined in the roadmap, the chip industry would have to add a manufacturing capacity of 250.000 wafers per month - the equivalent of three fabs the size Globalfoundries currently operates in Dresden. Would such a capacity translate into a predatory competition on a global scale? No, Wijburg said. “With such a production capacity we certainly would take away market share from Asia, but not volume” - the global demand would grow even faster.

For Joel Hartmann, Executive Vice President Manufacturing at STMicroelectronics, the initiative is perfectly in line with the company’s strategy. “This is a good opportunity to strengthen our R&D network”, he said. Marcel Annegarn, Director General of the AENEAS, the successor organisation of ENIAC, added a critical remark: “The report describes more a mission than a strategy”, he said. “There is much more funding, taxation and legislation needed,” he believes. In a meeting where business and technology should dominate, his remark called to the observer’s mind that after all the 10/100/20 program is still a political thing - and that the roadmap is not only driven by technology aspects but also by political desire.

So what will be the next steps for the European semiconductor industry? The industry will increase its R&D efforts - but this alone will not be enough, Wijburg pointed out. “R&D is important - it helps to create the next markets”, he said. But in order to achieve the goal or a stronger market share on a global basis, the entire value chain has to be strengthened. This will require massive investments”. Reinhard Ploss highlighted another important aspect: the technology and products that eventually will be created as a result of the program must be far enough ahead of the global competition to be safe from commoditizing. “Do we want to compete on low cost?” Ploss asked. “Certainly not”, he answered his rhetorical question. “This would not be a long-term successful strategy”. 

Infineon CEO Reinhard Ploss: “No competition on lowest price”

Globalfoundries Dresden CEO Rutger Wijburg: “Additional capacity of 250.000 wafers per month is needed”
Virtualization pushes into microcontrollers

By Nick Flaherty

VIRTUALIZATION IS SET to be the next battlefield for microcontroller technology. Both MIPS and ARM are bringing virtualization to industrial microcontrollers in different ways.

Imagination Technologies is rolling out the world’s first MCU cores that incorporate hardware virtualization, while ARM is preparing its own version of virtualization technology for the embedded market.

The MIPS M-class M51xx cores form the first group of entry-level MIPS Series5 Warrior CPUs for industrial control, Internet of Things (IoT), wearables, cloud computing, wireless communications, automotive, storage and other applications.

“With the MIPS Series5 M-class IP cores, we believe we’re bringing fresh thinking to the embedded world”, said Tony King-Smith, EVP marketing at Imagination.

“We have seen the trends leading to the need for more advanced multi-context security and multiple execution domains right across the CPU spectrum, which is why we are now rolling out virtualization across our entire range of MIPS Series5 CPUs, including the new entry-level M51xx family”.

The performance and low power credentials of our latest M-class CPUs have already generated a lot of excitement with our key licensees and partners, he said. With advanced functionality such as virtualization, full FUs and advanced DSP capabilities, complemented by mature tools both from ourselves and our ecosystem partners such as Mentor Graphics and Green Hills Software, were confident you’ll be hearing a lot more about MIPS embedded CPUs in the coolest and most disruptive chips and products.

Virtualization is also at the heart of the next version of the Cortex-R which was announced last October and is very much aimed at industrial customers who want the performance of microprocessor in a microcontroller, says Richard York, vice president of embedded CPU marketing at ARM.

We are still not ready yet to say what form the implementation will take but the construction of that has happened, he said. It needs to be thoroughly built before we talk to the world about it. We took that to companies such as Green Hills and they in particular have been great and crawling all over it with their virtualization hat on and they see it as spot on. It’s people like Green Hills that will make it a success or not if they can’t make their virtualization work it’s a non-starter.

“The M-class cores implement the MIPS Release 5 architecture incorporating hardware virtualization. The M51xx cores are based on the same 5-stage pipeline architecture and leverage the high performance, comprehensive digital signal processing (DSP)/SIMD features of the previous generation MIPS micro-Aptiv family of cores, along with the microMIPS Instruction Set Architecture (ISA) which provides up to 30% code size reduction over 32-bit only code.

The addition of hardware virtualization to MCU-class cores provides increased security and reliability for a wide range of applications allowing multiple, unmodified, operating systems and applications can run independently and securely at the same time on a single, trusted platform. This delivers a range of benefits for system development, including the ability to execute multiple tasks in isolation, intelligent resource allocation across several guests, secure downloads and uploads and IP protection.

Built-in prioritization mechanisms in the MIPS virtualization architecture, with support for up to seven secure/non-secure guests, enable it to optimally support real-time functionality. In space-constrained, low-power systems such as IoT or wearable devices, virtualization could be used to implement a multiple-guest environment where one guest running a real-time kernel manages the secure transmission of sensor data, while another guest, under RTOS control, can provide the multimedia capabilities of the system. For applications that demand an even higher level of security, the new M-class cores include tamper resistant features that provide countermeasures to unwanted access to the processor operating state. A secure debug feature increases the benefit by preventing external debug probes from accessing and interrogating the core internals.

The new M51xx cores also feature a Floating Point Unit (FPU) option supporting both single and double precision instructions for improved control systems processing. The FPU is well-proven, having been implemented in high-end MIPS cores.

Several hypervisors for the M-class cores are under development from Imagination and leading third party hypervisor developers, enabling customers to take full advantage of the hardware virtualization features. This includes several open source hypervisors such as KVM, the Kernel-based Virtual Machine, and a microkernel hypervisor, both of which are available now for the M5150 core.

The MIPS M5150 and M5100 cores are available for licensing now. Details of ARMs Cortex-R implementation are due later in the year.
One hardware, multiple domains: virtualising is the answer

By Christoph Hammerschmidt

AUTOMOTIVE HEAD UNITS increasingly are becoming the place where multiple application worlds and functional domains meet - from safety-relevant assistant systems to infotainment and internet access. Virtualisation, a software technique common in commercial IT and avionics, keeps these different data and software worlds securely separated.

Head units are the place where many data streams in cars meet. Here is the place where multimedia meets cloud computing, safety-relevant functions meet connectivity. An obvious solution to keep such a diversity of safety levels and functions separated would be to dedicate a hardware platform to each of them - but beyond prohibitive costs, also the space requirements in the anyhow cramped car cockpit prevent such a solution.

At Embedded World, automotive supplier Continental shows how such a problem can be resolved: the company designed a single common hardware platform that can run all these different applications with their unique set of requirements each, safely separated in their own virtual machine. The task of keeping these worlds apart is allocated to a hypervisor proven in aircraft systems, developed by software vendor Sysgo.

“The hypervisor technique allows us to run very different software worlds on a single hardware”, says Ralf Lenninger, head of Strategy and System Development at Continental. “This makes sense since through the increasing on-board and off-board connectivity the boundaries between the diverse cockpit applications are increasingly blurring”.

The platform runs Autosar software applications which need to meet high demand in terms of real-time capability, integrity and failsafe performance, such as an immobiliser or warning messages, along with Genivi-compliant infotainment applications which demand high computing power and memory space. Other applications on the same platform run in an Android environment, reflecting the needs of a digital lifestyle.

The Sysgo hypervisor partitions the hardware resources such as the computing power, memory space of a multicore processor into several virtual computers. Continental hides the complex software environment which also includes several displays under a common Human-Machine interface (HMI). The content of these applications are no longer associated to a dedicated display.

Instead, content assignment is flexible and follows situational requirements. “Depending on the driving situation, this information can be displayed in the instrument cluster, the head-up display, in the centre display or even on a connected terminal device such as a smartphone”, explains Torsten Posch, manager of Continental’s Software Technology Centre.

The company’s exhibit at Embedded World demos the functional integration of an instrument cluster, a Head Unit and an Android system on a common domain controller. As a part of Sysgo’s PikeOS real-time operating system the hypervisor provides three virtual machines running on one multicore microprocessor. Such a combination enables not only designers to run diverse applications with different safety and security requirements on a single hardware platform. At least as important as this is the possibility that it enables them to have different software life cycles coexisting on such a platform. It enables users to update dedicated software functions to keep pace with the market dynamics in the infotainment sector. The safety-reliant and long-lasting software remains unaffected.
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VTT develops printable e-nose sensor

By Julien Happich

SET UP AS A 3-YEAR research project, the European consortium PHOTOSENS achieved its original goal to develop low-cost, mass-producible polymer-based nanophotonic sensors for air quality, pharmaceutical process cleanliness and food safety applications.

Periodic optical nanostructures, known as photonic crystals when they affect the motion of impacting photons, can be implemented as nano-structured surfaces. Such nano-structured surfaces find use in so-called Surface Enhanced Raman Scattering (SERS) instrumentation, capable of characterising very accurately the chemical composition and structure of materials, in any state.

The surface-sensitive technique relies on precisely nano-engineered structures plated with gold, which have the effect to enhance transitional Raman photon scattering at a set of frequency bands unique to each material (like a signature of its chemical composition and state).

Until recently, such nanophotonic structures were difficult or expensive to manufacture in large volume. This challenge was addressed by the Photosens consortium using roll-to-roll (R2R) nanoimprinting methods. The photonic crystal sensor was demonstrated first at wafer level then at sheet-level using tailored polymer materials – see figure 1.

Fig. 1: Photonic Crystal structures replicated into a polymer material.

Nanoimprinting, also known as nanoimprint lithography (NIL) consists in pressing a micro-structured mold against a substrate coated with a moldable material. After deformation of the material, the coating is UV-cured and the mold is separated to leave a perfect replica.

Of course the initial mold could be engineered through optical lithography, but in this case it was provided by commercial partner 3D AG in the form of a nickel shim recombined from various masters structured using electron-beam lithography. Then the shim was attached onto a reel for the roll-to-roll UV imprinting machine to manufacture the nanophotonic sensor structures at high-throughput, in effect, nano-texturing large-area plastic films – see figure 2. Special polymer materials were also developed, including functionalized molecularly imprinted polymers (MIP) to optimize sensor sensitivity.

Fig. 2: UV R2R nanoimprinting process

Roll-to-roll printed polymer SERS structures and gold coated SERS chips with two different form factors.

Project Coordinator and Research Professor for Photonics Solutions at the VTT Technical Research Centre of Finland, Dr. Pentti Karioja explained EE Times Europe that even with a sensitivity of an order of magnitude lower than the commercial reference, the photonic crystal sensors obtained have the potential to meet the initial target of formaldehyde detection in air. Formaldehyde is a common indoor air pollutant found in virtually all homes and buildings.

Using a R2R process on roll batches 400m long by 0.3m wide, sensor chips could be mass produced in tens of thousands of units costing less than €1.5 each. For the SERS sensor, a gold metallization further enhances the Raman scattering effect. At the moment, this would drive the price up to around 3€ per individual sensor, but it could be driven lower using R2R metallization.

Further material and process optimization could still lower cost.

Functionalized nano-structures could be tailored to detect specific chemical compounds, to build multiple gas sensing chips at much lower cost.

Disposable SERS sensor and photonic crystal sensor readout concepts were elaborated by the consortium. The SERS sensor can be read out using a commercial Raman reader, which is still quite an expensive instrument, but for the photonic crystal sensor, a table-top readout unit was developed using a commercial CCD camera and a fiber pigtailed laser source.

This way, the disposable polymer chip is placed in a cartridge for easy and repeatable alignment of the sensor chip with the excitation laser and CCD readout. A waveguide sensor based on the Young interferometer principle was also manufactured using the R2R process, read out by a similar type of reader which would be about ten times cheaper than conventional Raman readers.

Other partners in this project included the University of Southampton (UK), Momentive (Germany), TNO (the Netherlands), University of Vienna (Austria), Nanocomp (Finland), 3D AG (Switzerland), Philips (the Netherlands) and Renishaw Diagnostics (UK).
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Google prototypes depth-sensing mobile phone

By Peter Clarke

OMNIVISION, MOVIDIUS and Paracosm could benefit if Google can hone its just announced prototype depth-sensing mobile phone.

Google has announced that it has developed a prototype Android 5-inch mobile phone that includes a depth sensor alongside a motion-tracking image sensor.

The phone is the result of a one-year R&D initiative called Project Tango, and according to material at the Google website this 3D-tracking phone could provide a solution to location mapping and tracking as well as being a platform for new types of games and for robotics applications.

The company says it will hand out part of an initial build of 200 prototypes of the phone to software developers for them to develop applications on. “We want partners who will push the technology forward and build great user experiences on top of this platform,” said Google on its website.

The current prototype is a 5-inch mobile phone with custom hardware and software designed to track the unit’s 3D motion and map its surroundings.

Source: Google

Google prototypes depth-sensing mobile phone

![Fig. 1: The 5-inch mobile phone prototype with custom hardware and software designed to track the unit’s 3D motion and map its surroundings. Source: Google](Image)

IBM sets data transfer record in multimode optical fiber

By Jean-Pierre Joosting

BY SENDING DATA at a rate of 64 Gb/s over a cable 57 meters long using a vertical-cavity surface-emitting laser (VCSEL), researchers at IBM achieved a rate that was around 14 percent faster than the previous record and about 2.5 times faster than the capabilities of typical commercial technology.

To send the data, the researchers used standard non-return-to-zero (NRZ) modulation. “Others have thought that this modulation wouldn’t allow for transfer rates much faster than 32 Gb/s,” said researcher Dan Kuchta of the IBM T.J. Watson Research Center in New York. Many researchers thought that achieving higher transmission rates would require turning to more complex types of modulation, such as pulse-amplitude modulation-4 (PAM-4).

“What we’re showing is that that’s not the case at all,” Kuchta said. Because he and his colleagues achieved fast speeds even with NRZ modulation, he added, “this technology has at least one or two more generations of product life in it.” Following this achievement it is expected that standard, existing technology for sending data over short distances should be able to meet the growing needs of servers, data centers and supercomputers through the end of this decade.
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AN AUSTRalian COMPANY claims to be edging closer to creat-
ing the capability to print ‘light-effects’ directly on paper and
cardboard using electroluminescence technology. The result
could include flashing lights on packaging, illuminated maga-
zine covers and books with ‘highlighted’ areas.

prelonic, a company founded by entrepreneur, Dr. Friedrich
Eibensteiner, is well advanced in the development of the elec-
troluminescent lamps (EL) technology to enable the printing of
‘light-effects’ directly onto paper and cardboard via convention-
al printing processes working in a normal printing environment.

Dr. Eibensteiner believes electroluminescence still seems
to be the only light technology which can be printable and will
be available in the next years with reasonable effort. Although
LEDs are available Dr. Eibensteiner points out that they are not
printable and they still require pick place processes. LEDs also
only produce small light spots – even if they are robust and
bright. OLEDs offer area lighting, but are not suitable for the
printing applications for anumber of reasons including the need
for clean room processes, encapsulation and high costs.

Full development and roll-out of EL printing on paper will
take some time admits Dr. Eibensteiner but he reckons after that
a cost efficient technology for lights on magazines, books and
packaging will be available.

prelonic expects the first EL printing applications will be
hybrid ones because the driver is still not fully developed. But
prelonic has realized a solution that now enables printing by
using most of the driver components which can be completed
with few simple conventional printing functionalities.

The hybrid approach could enable conventional screen print-
ing in a normal paper and cardboard environment to be achiev-
able which is a pre-condition for low cost mass production.
Flexible OLED lighting demonstrators, 50µm thin

By Paul Buckley

THE UK’S CENTRE for Process Innovation (CPI) has unveiled a range of flexible Organic Light Emitting Diode (OLED) demonstrators.

The devices, which have been manufactured on CPI's OLED/OPV Prototyping Line, have been built on a range of substrates with thickness ranging from 50 µm to 125 µm.

The device structure consists of an Indium Tin Oxide anode, evaporated hole injection layer, co-evaporated emissive layer and a conventional cathode. The device chemistry can be modified to produce a variety of colors and is encapsulated using a pressure sensitive adhesive and a commercially available barrier material.

CPI's prototyping line has been designed to enable the development and production of organic light emitting diode and organic photovoltaic technologies.

Located within CPI's state of the art ISO Class 5 clean room facility, the prototyping line provides materials companies, device designers and end users with the opportunity to develop their technology within an automated and closely controlled environment.

CPI is also investigating a number of methods for device encapsulation and is collaborating with adhesive, getter, and barrier film suppliers to produce robust manufacturing processes aimed at maximising lifetime and device performance. Work is being carried out via collaborative programmes OLAE + (Flexibilis) and TSB (HiPBE) to produce prototypes for the characterisation and development of high performance barrier layers.

CPI's technology roadmap is targeted at advancing the development of flexible optoelectronic devices and to address many of the challenges encountered in scaling up emerging technologies to commercialisation by adopting roll to roll processing techniques.

CPI plans to further enhance its capability with the installation of a 300 mm web roll to roll (R2R) coater for the printing of a range of organic material sets. The system will include both slot die and screen printing capabilities, with options to upgrade to 500mm web width and to incorporate other printing techniques such as reverse gravure. CPI will also install an encapsulation module allowing devices manufactured within the roll to roll coater to be laminated using a barrier film, thus providing protection to the device from water and/or oxygen ingress, both of which are detrimental to device performance and lifetime.
Piezo-nanowires boost fingerprint resolution

By Julien Happich

WITHIN THE 3-YEAR €2.9M EU Commission funded PIEZOMAT project (PiezoMAT), CEA-Leti and seven other European partners are joining forces to explore the use of piezoelectric ZnO nanowires in fingerprint sensors.

This stems from earlier research at CEA-Leti, demonstrating the potential of such nanowires to form very sensitive sensors or to collect piezoelectric charges for energy harvesters. In a paper published in 2012, researchers from CEA-Leti were characterizing the sensitivity of vertically grown ZnO nanowires on a silicon substrate, distributed in a pixel configuration through appropriate seeding layer patterns and metallic electrodes.

A research engineer at CEA-Leti and one of the co-authors, Emmanuelle Pauliac-Vaujour told us more about the PiezoMAT project.

“We have already proven the high sensitivity of ZnO nanowires for pressure detection, and with this new project, we aim to harness each nanowire as a pressure point (a pixel) for what would be a very high resolution fingerprint sensor”, said Pauliac-Vaujour in an interview with EETimes Europe.

Nowadays, state-of-the-art commercial fingerprint sensors don’t go beyond 1000DPI in resolution (dot per inch), and a resolution of 500DPI is the current international standard for compliance with the U.S. Federal Bureau of Investigation automated fingerprint identification systems. As an example, a 12.8x15mm fingerprint sensor with a resolution of 508DPI translates into 256x300 pixels that are 50µm by 50µm each. By comparison, using a single ZnO nanowire for each pixel (with a diameter of 0.5µm and 6µm long) could yield fingerprint sensors of pixel sizes well under one micron square, translating into resolutions up to hundreds of times higher, featuring up to a hundred million pixels. Those fairly “large” nanowires would be used because they would be easier to connect to a chip. But ZnO nanowires can be grown with much smaller diameters, it is just a matter of patterning finer nucleation windows in poly(methylmethacrylate) coated ZnO surfaces.

“If we can demonstrate fingerprint sensors based on pixels under a micron square, this will already be a huge competitive advantage” said Pauliac-Vaujour, adding that having French industrial partner Safran Morpho onboard the project had been key to secure European funding. A supplier of authentication solutions and biometrics, the company will help define the specs of the demonstrator for commercial applications. It will also be able to validate the sensor concepts with its own fingerprint capture and analysis algorithms.

“We’ll first explore this new concept on a silicon base, because this is where the read-out electronics will be integrated, and we figured out that if we use a die of similar size to exist-

Both the Kaunas University of Technology (Lithuania) and the Tyndall National Institute (Cork, Ireland) will contribute with multi-physics models at different scales. Another research partner, Fraunhofer IAF (Freiburg, Germany) will characterize each steps of the fabrication process.

What is there to see above 500DPI?
Surely Safran and other manufacturers are racing for higher pixel densities, as a sales argument. But does this imply that existing 500dpi solutions are prone to errors in fingerprint matching and to what extent would this error rate be reduced?

In other words, what is the relationship between fingerprint matching error rate and pixel

SEMP image of a highly ordered ZnO nanowire array grown on poly(methylmethacrylate) (PMMA) templates. R. Erdelyi et al., Crystal Growth and Design vol. 11, pp.2515-2519 (2011).

Fig. 2: The PiezoMAT fingerprint sensor concept showing vertically aligned interconnected ZnO nanowires, each constituting a single pixel of the sensor.
IBM Begins US Layoffs

Jessica Lipsky

IBM BEGAN ITS FIRST round of United States layoffs Thursday as part of a “global rebalancing” act that could save about $1 billion in costs. The restructuring process could see as many as 15,000 jobs being cut globally, including India, Brazil, and the European region.

Charles King, principal analyst at Pund-IT, told EE Times:

“The company has been undergoing a pretty elemental shift in its businesses over the last five to 10 years. IBM was mainly a hardware provider with a lot of attached services, has become a software provider with associated hardware. As the popularity of platforms waxes and wanes, they let workers go in divisions that aren’t as profitable as they used to be and hire new positions they believe will be more successful.

Poor fourth quarter numbers, a 26% slump in hardware revenue, and various divestments have fueled layoffs. According to Alliance@IBM, an IBM employee organization, an unknown number of layoffs have occurred in Massachusetts, New York, Iowa, Missouri, Oklahoma, North Carolina, Minnesota, Arizona, and Vermont.

Layoffs have already occurred in Bangalore, India, where unofficial estimates show 1,000 jobs lost. No official numbers were immediately available on IBM’s US employees. King said:

When a product division like [IBM’s low-end server business] is sold off, what you’ll see is firings in the marketing and sales divisions; the business unit is slowing down and getting ready to be owned by someone else. And a lot of times, the people below managerial level are often the ones that feel the pain first.

Alliance@IBM reported 10 to 15 jobs lost in Endicott, N.Y., while the Burlington Free Press reported that downsizing in Essex Junction, V.T. is expected to be about 140 jobs -- about one third the size of last year’s 419-person cutback. The Poughkeepsie Journal noted at least three local jobs had been cut from the Systems and Technology Group, which works on development and manufacturing of mainframes and other large computers.

“The company, in a departure from past practice, has even left out some pages from its packages given to employees that let a person figure out the size of the downsizing in a given business unit,” the Journal continued.

IBM officials did not return calls for comment.

“This magnitude of layoffs is something we’ve seen over and over again at other IT vendors. HP in particular has gone through some pretty devastating layoffs,” King said, adding that he does not think layoffs will have much effect on IBM’s market status. “I think, unfortunately, this is the kind of strategic headcount reduction that happens very often as technologies come and go and vendors try to respond to changes in the market.”

Jessica Lipsky, Associate Editor, EE Times

Fig. 3: Finite element calculations for the PiezoMAT concept using COMSOL Multiphysics: (a) Side view of a microfabricated pixel; (b) 3D representation of the simulated pixel; (c) Meshing and boundary conditions; (d) Profile of the piezoelectric potential generated within the bent nanowire (A) and the collecting electrodes (B) for a nanowire 600nm long with a 25nm radius.
By Peter Clarke

MAXIM INTEGRATED'S CEO, Tunc Doluca takes a few questions from EE Times Europe on analog, MEMS and the company’s strategy for the future.

EE Times Europe: How would you characterize the differences between Maxim under your predecessor Jack Gifford and under yourself?

Tunc Doluca: I worked with Jack Gifford for many years and respected him greatly. An effective teacher, he had passion, intellect and brilliant ideas. He drove people hard to deliver results, but he also rewarded them. I became CEO in 2007 and, although we have made several changes (such as centralizing our supply chain to better serve our customers and reorganizing to focus on end markets), we continue to execute on Maxim’s vision of creating highly integrated products. That started under Jack; it is not new for Maxim Integrated. In fact, we modified our company name in 2012 to underscore that focus and expertise. We accelerated the changes to adapt the company to our strategy.

EE Times Europe: Is it a move away from analog building block products and towards mixed-signal solutions including software? And some digital-only solutions?

Tunc Doluca: Maxim has built a leadership position in analog and mixed-signal integration. We continue to grow operational excellence and revenue in areas such as multi-chip system-in-packages and fully integrated mixed-signal SoCs. While highly integrated products, which now comprise about half of our revenues, are our differentiator, we continue to create great building-block products. That will never change. Over time, we have built a rich portfolio, which grows to this day. These ICs showcase our innovation, are successful in the market, and help our customers differentiate their systems. Ultimately, many of our standalone products will emerge as candidates to be integrated with others onto a chip. However, some of these products will remain clever, best-in-class discrete components.

EE Times Europe: Is it more application and market oriented? In which case what are Maxim’s markets and what characterizes them in terms of volumes, ASPs, etc.?

Tunc Doluca: In 2011, we reorganized to focus on end markets so, yes, I would say we are market-oriented. Driven by demand for smartphones, mid-range phones and tablets, our mobility business grew the fastest. It is currently the largest segment in terms of revenues. As smaller form factors and power efficiency become more critical, we target other applications that can benefit from our expertise in analog integration. These include smart meters, automotive infotainment and portable medical equipment. However, we value and target the broad market, too, primarily small and medium-sized customers in the industrial space. Our business model effectively balances high-growth mobility with the stability and long term annuity of the industrial and communications markets.

EE Times Europe: Where do you manufacture and what is the strategy?

Tunc Doluca: Several years ago, we centralized our supply chain operations. That enabled us to better serve our customers and realize efficiencies. To provide flexibility and additional capacity, our hybrid manufacturing model has served us well. Our internal wafer fabs are located in the U.S. — San Jose, Calif., San Antonio, Texas, and Beaverton, Oregon. Our test and assembly sites are in the Philippines and Thailand. We engage foundry partners to augment our internal facilities, and about half of our products are made at partners’ fabs using Maxim’s unique process technologies. These are true partnerships, not simple outsourcing.

EE Times Europe: I think under Jack a number of mature manufacturing facilities were acquired right up until 2007. Under yourself none! Are you becoming more fab-lite over time?

Tunc Doluca: Keeping some manufacturing in-house differentiates us from our fabless competitors because in analog, there are specialty technology requirements. We designed our hybrid manufacturing model — i.e. using a blend of internal fabs and foundry partnerships — to flex according to demand and market needs. It is working very well for us; I do not anticipate it changing.

EE Times Europe: You have a proprietary process technology at 0.18-micron but what about mixed-signal at 90nm, 65nm, 28nm. Do you rely on foundries for that?

Tunc Doluca: While we utilize our foundry partners to manufacture products on some of the smaller-geometries, they are using Maxim’s proprietary process technologies. As a result, we continue to heavily invest in this area. Obviously, we do not publicly discuss “which specific process technologies are where.” However, I can tell you we have qualified and are ramping several leading-edge analog processes in our own fabs. Several product lines require deep sub-micron technologies and for those we utilize merchant foundry process at and below 65nm.

EE Times Europe: What is the role of MEMS and other sensors at Maxim? Do you have all the building blocks for wireless sensor networks? Internet of Things?

Tunc Doluca: Sensors are a critical adjacent function to analog semiconductors, and the sensor market is expected to grow rapidly as new applications emerge. Through both internal development and acquisitions, sensors and MEMS have an impactful role at Maxim. While our gesture sensor in Samsung’s Galaxy S4 received considerable attention, we are actually investing, developing and manufacturing sensors for numerous applications and markets. In fact, very few semiconductor companies have touch, motion/ MEMS and optical sensor technologies in their portfolios. We have all three. It is possible to fuse various types of sensors with our analog technology, enabling all sorts of applications, including the Internet of Things and wearables.... 

Tunc Doluca, Maxim Integrated’s CEO

Since the mid-1980s, we have been working with the Internet of Things (IoT) as an adjacent market. We have a rich portfolio, which grows to this day. These ICs showcase our expertise in analog integration. These include smart meters, automotive infotainment and portable medical equipment. However, we value and target the broad market, too, primarily small and medium-sized customers in the industrial space. Our business model effectively balances high-growth mobility with the stability and long term annuity of the industrial and communications markets.

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Tunc Doluca, Maxim Integrated’s CEO

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ARM’s server platform standard to ease OS interoperability

By Julien Happich

ARM’S RECENT ANNOUNCEMENT of a collaboratively developed platform standard for ARMv8-A based (64-bit) servers comes after years of consensus across many partners, three years after the first specifications of the ARMv8-A 64-bit architecture were announced, and about a year after the actual IP was made available.

During all that time, ARM worked closely with OS and firmware vendors such as Canonical, Citrix, Linaro, Microsoft, Red Hat and SUSE, but also OEMs including Dell and HP along with silicon partners such as AMD, Applied Micro, Broadcom and Texas Instruments. “We’ve put the specs out for people to review and question, under non-disclosure agreements”, said Jeff Underhill, Director for Server Programs at ARM when talking to EE Times Europe. “This was still a forward looking activity, with discussions on IP that was not yet in the public domain”, Underhill added.

The goal of the ‘Server Base System Architecture’ (SBSA) specification is to provide a framework with all the common blocks defined at SoC-level, in order to accelerate software development and ease OS and firmware portability across ARM-based platforms.

In effect, the SBSA sets the minimum hardware requirements and ensures that all the platform hardware (including heterogeneous elements) is describable or discoverable. It also defines platform virtualization.

“Basically, all agree to have watch dog controllers and timers, virtualized interrupts and IOs, performance monitoring units, things that an OS need to boot out of the box. So let’s agree on the way we do that so OS and firmware vendors can make their products portable across all the ARM platforms, irrespective of which OS variant they offer”, said Underhill.

“You are still free to innovate beyond the basic specs. Silicon vendors can bring their value-added components, for example more advanced features such as accelerators, and we don’t want to lock that down. But make sure that they are discoverable by any OS through the same mechanism”, he clarified.

The enterprise server space is relatively new to ARM, conceded Underhill, but ARM has a healthy alignment with the networking space. “We estimate that the total available market (TAM) of servers will grow 30% by 2017 and we expect to capture between 5 and 10% of that TAM with the SBSA”. By 2020, 25% of servers could be ARM-based, according to industry analysts.

“As ARM’s data center ecosystem continues its rapid growth, this milestone enables partners to focus on their innovation while building on standards that help simplify their development and accelerate their time-to-market,” said Mike Muller, ARM’s chief technology officer in a statement.

At the Open Compute Summit a few days ago, partner AMD has announced a comprehensive development platform for its first 64-bit ARM-based server CPU, fabricated on a 28nm process. The company also announced its contribution to a new micro-server design using its AMD Opteron A-Series processor codenamed “Seattle” and due to sample this quarter.

Other partner, Applied Micro, has announced X-Gene 2, expected to sample in spring 2014 as the world’s first ARMv8 scale-out Server-on-Chip.

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Implantable hearing aid boasts wireless charging

By Julien Happich

AT THIS YEAR’S IEEE International Solid-State Circuits Conference, MIT researchers have presented a paper on fully implantable hearing aids that would not require any connection to an external apparatus for operation.

In their paper “A Fully-Implantable Cochlear Implant SoC with Piezoelectric Middle-Ear Sensor and Energy-Efficient Stimulation in 0.18µm HVCMOS”, the researchers detail the design of a middle-ear implant that converts the vibrations of ossicles in the middle-ear into electric signals fed to the cochlear (a small spiral chamber in the inner ear) through micro-electrodes.

Demonstrated with measurements from human cadaveric temporal bones, the solution relies on a system-on-chip specifically designed to interface to a piezoelectric sensor, itself mounted at the umbo of the malleus within the middle ear, explains the paper. The IC also features a highly-reconfigurable digital sound processor that supports system power scalability through audio spectral channel selectivity. It also integrates neural stimulation via eight commercially available micro-electrodes.

First, a piezoelectric sensor frontend (PZFE) conditions the signal from the sensor (the sound-induced motion of the umbo), the signal is digitized by a low-power SAR ADC before a reconfigurable sound processor implements continuous interleaved sampling (CIS). Research indicates that the speech recognition scores of cochlear implant users improve with the number of electrodes but plateaus after 7 or 8, hence for the demonstrator, it was decided that the number of channels could be reconfigured between 8, 6, or 4 to enable a power-performance trade-off. All processor parameters are programmable to enable a patient-specific fit, indicate the authors. Finally, a neural stimulator is implemented with a single current source interleaved among all electrodes at 1000 pulses/s per electrode while a high-voltage switch matrix selects the active electrode.

Key to making this battery-operated implant workable (with a very small battery) was the development of a new signal-generating circuit that could further reduce the chip’s power consumption. For this purpose, the researchers specified a new waveform modulation scheme to encode the acoustic information in a very power-efficient way that can still stimulate the auditory nerve in the appropriate way.

In this exercise, MIT’s Microsystems Technology Laboratory (MTL) Professor Anantha Chandrakasan who specializes in low-power chips, had to tailor the arrangement of low-power filters and amplifiers to the precise acoustic properties of the incoming signal.

“One way the implant could be wirelessly recharged would be at night through a special pillow that the user sleeps on. Another way would be through a portable device, for example a cell phone that recharges the implant in the amount of time it takes to make a phone call” explained the paper’s lead author Marcus Yip who completed his PhD at MIT last fall.

“In either case, we use magnetic resonance to transfer power between a pair of coupled coils, one in the transmitter and one in the implant receiver”, Yip added.

The researchers have already designed a wireless charging controller chip and the associated circuits that complement the implant, to recharge it in roughly two minutes. Two of their collaborators at Massachusetts Eye and Ear Infirmary (MEEI), Konstantina Stankovic, an ear surgeon who co-led the study with Chandrakasan, and Don Eddington, tested it on four patients who already had cochlear implants and found that it had no effect on their ability to hear...
Automated driving demonstrated at Mobile World Congress

By Christoph Hammerschmidt

The vehicle at the Mobile World Congress is the result of more than ten years of corporate research dedicated to automated driving functions and will be used to further develop sensors and driver assistance systems for next-gen vehicles. With the platform, the carmaker intends to fathom out technological issues associated to automated driving as well as legal and societal ones.

The trial vehicle uses a rotating Lidar (Light Detection and Ranging) sensor located on the roof to scan the surroundings with a range of some 70 metres (230 feet). According to Fort, the sensor can identify vehicles, pedestrians, bicycle riders and even small animals. The data generated are transformed in real-time into a virtual 3D map that contains all the objects detected with direction and distance to the vehicle. During the development of the vehicle, Ford collaborated - among others - with the University of Michigan and US insurance group State Farm.

While the work of the university scientists focused on the development of the sensors and control computers, the collaboration with the insurance company aimed at evaluating the chances and risks of autonomous driving.

In 2014, Ford launched two new research projects in the US designed to deepen the understanding of autonomous driving. In collaboration with the Massachusetts Institute of Technology (MIT), Ford tries to find out how a vehicle can predict the movement trajectories of other traffic participants including pedestrians by means of innovative algorithms. At the same time, the carmaker develops solutions how vehicles can circumvent obstacles to keep the further traffic development in sight; this project is conducted along with the Standard University.

In Europe, Ford collaborates with the Aachen Technical University RWTH in developing innovative HMI concepts. Ford assumes that HMI design is a crucial component to implement autonomous driving since they bundle the entire interaction between vehicle and driver. This is an important factor since the driver must be able to resume the control over the vehicle in very short time, if necessary.

The Ford test platform, based on a series Focus vehicle, also contains a number of advanced driver assistance systems such as a parallel parking assistant, automatic city stop or voice control for audio systems, air conditioning and navigation system. For the design of the platform, Ford utilised the results of its "Driver in Control" analysis, conducted on the company’s Virtual Test Track Experiment (VIRTTEX) driving simulator.
SMPS: a crucial component of the “system Data Center”

By Francesco Di Domenico

Improving the standard of living requires ever-increasing demand for energy, particularly in electrical forms. People do not use directly electrical energy, but mainly IT and telecommunication equipment, transportation vehicles, white goods, light, mechanical work or media: these are all the tangible effects of the electrical energy.

Power electronics is the science studying the ways to convert electrical energy into the forms typically used in the daily life. A modern power conversion system consists of an energy source, an electrical load, a power electronic circuit, and control functions: the control circuits take information from source and load, determining how the switches must operate to achieve the desired conversion.

This is exactly the principle of operation of the SMPS (Switch Mode Power Supply), which uses a high frequency switch (in practice a transistor) with varying duty cycle to maintain regulated output voltage.

An AC/DC SMPS is a system consisting of three main stages, as shown in figure 1 in the case of a typical IT server application.

In each of these 3 stages the role of power or logic components based on semiconductors is fundamental: high voltage power MOSFETs, diode and controllers in the PFC and PWM/resonant stages, Low Voltage power MOSFETs or diodes in the rectification stage.

More recently the focus has been moving from a "device-driven" to an "applications-driven" scenario, in a "system engineering" approach. This transition has been mainly triggered by the fact that advanced semiconductors with suitable power ratings already exist for almost every application of wide interest, so designers show an increasing interest in a more flexible, reliable and of course efficient way to use them.

According to the new “system” approach, efficiency and power density are definitely more and more in the focus of SMPS design, especially in IT computing applications. Figure 2 shows the most popular efficiency standard followed in this environment, the 80Plus, which fixes the minimum efficiency requirements in typical operating condition (20, 50 and 100% loading).

The most recent one, the Titanium, imposes the requirement even at 10% loading, so at very light load: this is consistent with the operation of modern computing systems, where each power supply is typically used in a paralleled N+1 redundant configuration, so it will work most of the time at load much closer to 10% than to 100%.

In fact in the past the increasing efficiency need was mainly driven by the capability of heat dissipation at full load without excessive impact on fan’s acoustic noise generation: as a result, maximizing the full load efficiency was more in the focus.

However, more recently the explosive growth of consumer electronics and data processing equipment had pushed to the introduction of various requirements aimed at the optimization of light-load operation. For example, the workload of Web services can significantly vary based on diurnal cycles, application weights, external events, etc. And this is mostly valid even for High Performance Computing (HPC) and cloud servers.

Meeting this stringent light-load efficiency poses major design challenges to power supply manufacturers and huge effort has been dedicated by both power semiconductors and control ICs providers in developing technologies able to comply with these specifications and making SMPS efficiency plot as much as possible “flat” in the entire load range.

A modern data center looks like an array of racks; in each “drawer” of it we find a server, and in each server a SMPS can be found – see figure 3: therefore a large number of power supplies are expected to be inside such a structure.

Looking at the diagram of the power delivery system of a typical large server farm, for each Watt consumed by data processing, more than two Watts are wasted in power conversion and cooling.

An important parameter used to quantify the server efficiency inside a data center is the so called Total Cost of Ownership (TCO), defined as the cost to equip and run the servers. In fact, TCO consists of two main components, the CAPEX (Capital Expenditure, so equipment costs) and the OPEX (Operating Expenditure, so the energy cost). With steadily decreasing prices of IT equipment, the cost of electricity over the equipment lifetime has become a significant fraction of the initial acquisition cost, especially for low-end equipment such as “blade”, 1U, and 2U servers (where “U” is a unit of height measuring 1.75 inches or 4.45 cm), where the cost of power and cooling is...
exceeds the acquisition cost in approximately three years. As a result of the increasing impact of energy cost on the TCO, efficiency considerations have started to have a significant influence on equipment acquisition decisions, starting of course from the SMPS selection.

In addition, the increasing power consumption of IT equipment and in particular that of fast-growing large data center facilities has started to have a serious environmental impact, especially in terms of CO₂ emission.

A third important component affecting the TCO is the reliability of components, since repairs can be costly in labor and reserve-capacity provisioning. A similar but maybe less tangible element affecting the TCO is the serviceability of the servers, which involves the time, and therefore the cost of repairs and upgrades. The size and weight of the components, especially the SMPS, may significantly influence this parameter. For this reason the trend in increasing efficiency goes hand in hand with the increasing power density. Figure 4 gives a short overview of the specific impact on SMPS requirements.

In fact, SMPS did not see a dramatic change in power density until the beginning of the rapid growth of the Internet: while a typical power density of server front-end power supplies was in the 10 W/in³ range just 10 years ago, the power density requirement is today in the 40 W/in³ range. As this trend continues, SMPS with more than 50W/in³ will be commonly available in few years. These dramatic power density gains have been primarily enabled by the availability of better components (both semiconductors and magnetics), advanced packaging techniques, but also design optimization and consequent new advanced control techniques.

An important contribution to the future efficiency and power
density is expected to come mostly from system architecture and power management optimization. For this reason, the digital power management bus has been already standardized by the PMBus Consortium. In addition to PMBus compliance, digital control techniques become increasingly popular in power conversion.

Generally, while digital power management can optimize performance at the system level, digital control contributes to optimize the converter-level efficiency in the entire load range by implementing adaptive, load-dependent control algorithms, or phase-shedding in interleaved structures in order to achieve almost flat efficiency plots. In addition, within the digital control, monitoring, protection, and house-keeping features of power are shifted from hardware to software, which significantly shortens product design time, reduces the cost, and also allows for easy adjustment (“tweaking”) of parameters even during the mass production.

Regarding the circuital topologies used inside SMPS, the opportunity to significantly reduce the size of power converters by increasing the switching frequency created by the MOSFET technology has focused topologies studies on the reduction of switching losses of the semiconductor devices, which is typically perceived as the major obstacle to maximizing the switching frequency of PWM converters. This has given big emphasis to the resonant power conversion, which led to the development of new families of resonant converters, based on the zero-voltage-switching (ZVS), zero-current-switching (ZCS), quasi-resonant (QR) and multi-resonant concepts.

From what is mentioned above, the role played in SMPS advancement by semiconductor companies like Infineon looks really crucial: power devices, drivers, ICs, analog and digital controllers, everything inside Infineon portfolio, are all fundamental parts of such a system. For this purpose, figure 5 shows the typical internal structure of a Server AC/DC SMPS and the several families of Infineon components which are used in each of its stages.

In fact, the outstanding improvements in SMPS performance achieved in the past 10 years have been primarily brought by the dramatic reduction of the on-resistance achieved in high-voltage MOSFETs using the revolutionary Super Junction principle, introduced by Infineon at the end of the nineties in the CoolMOS™ series and equally impressive improvements in reverse-recovery characteristics of high voltage SiC (Silicon Carbide) diodes. In applications with a low output voltage, further efficiency improvements have been made possible by continuous reduction of on-resistance of low-voltage MOSFETs, like Infineon OptiMOS™ series, used as synchronous rectifiers. Introduction of innovative devices based on GaN (Gallium Nitride) material promises further revolutionary advancements in this field.

An important contribution to the progress of SMPS technology comes in particular from the packaging techniques, having the main goal of minimizing parasitics and improving thermal performances. The need of increased power density has been also triggering more and more advanced component integration: monolithic integration and/or chip co-packaging of semiconductor components such switches, drivers, and control circuits looks promising in order to shrink the system size. For the same reason the use of magnetics with integrated PCB winding(s), allowing more functional integration, will find more extensive use.

Unfortunately, it is commonly recognized that the fast progress in semiconductor technologies has been not followed at the same pace by magnetics and capacitors technology. The major effort of magnetics manufacturers has been focused on the optimization of the existing materials in certain frequency ranges and expanding the portfolio of core shapes and sizes, in particular low-profile planar cores, which is surely helpful for the designers. However, more innovative solutions would be needed in order to further minimize the copper losses due to skin and proximity effects, still considered as the actual major trouble in high-frequency applications. Finally, some progresses have been made in the field of low voltage capacitors technology, but no significant changes have been introduced in the high-voltage electrolytic capacitors used as energy-storage (bulk) capacitors: in fact, despite the introduction of some miniaturized series, their typical capacitance/volume ratio is still relatively low.
Wireless charging shift ahead

By Jessica Lipsky

At least four different approaches to wireless charging are vying to power billions of next-generation mobile devices. Today only one has a beachhead in about a million systems: the Wireless Power Consortium's Qi inductive charging technology.

By 2018, analysts say, the race will be all but over with one player dominating the 700 million systems using wireless charging. Experts expect a technology shift to resonant charging after a generation of hybrid inductive/resonant products currently coming on the market. Before it’s over, Apple is expected to debut what could be a wild-card proprietary approach.

Wireless charging “standards have to converge, and I think this year they will figure out this market is not taking off until they get together,” Henry Samueli, the chairman and CTO of Broadcom, said at a company event in December in San Francisco. “It’s about much more than a smartphone market. The main driver is the Internet of Things.”

Fig. 1: ConvenientPower's dual-mode inductive/resonance multi-device charger. (Source: WPC blog)

Ryan Sanderson, a wireless charging analyst at IHS, told us the mobile phone and tablet markets will be key to volume adoption of wireless charging in the coming years. IHS forecasts assume that at least one major cellphone manufacturer will integrate wireless power capability throughout its ecosystem by 2016.

“Apple is probably not eager to adopt another standard for it. They’ll want to develop their own thing. They have a huge influence, along with Samsung,” IHS analyst Jason dePreaux told us. “It will take those two companies to create a standard, not just saying the standard or joining an alliance, but actually building it in. It’s several years away, though, especially on the Apple side.”

Three types of main wireless charging technologies are contenders in the race to mainstream use - magnetic induction, magnetic resonance, and niche solutions such as radio frequency. Though dePreaux said there isn’t much difference in power or charging time among the technologies, an Ars Technica speed test of the Qi (pronounced chee) technology showed that

Jessica Lipsky is Associate Editor of EE Times - www.eetimes.com
charging a Google Nexus 7 wirelessly took nearly three times as long as using a power adapter.

Trade groups of chip makers and patent holders back different charging platforms. The Wireless Power Consortium (WPC) backs inductive and bridge solutions, while the Association for Wireless Power (A4WP) champions resonance. Seeing the writing on the wall, the Power Matters Alliance has moved to embrace resonant charging, as well.

The startup Humavox is going it alone with an approach that is based on what it calls radio frequency charging. Still, market watchers say other players and technologies could emerge before the dust clears.

“In the future, it’s possible that technologies which offer the consumer even more freedom of space and distance to charge wirelessly - RF perhaps being an example of this - will enter the market and compete with resonant technologies,” Sanderson said. Advancements are likely several years out. “In my opinion, it will be difficult for a new technology to enter the market once an infrastructure is in place, and therefore, if one technology is adopted in volume in the next two years, it is likely to remain the technology of choice for the future.”

Last year, 20 million wireless charging receivers were shipped, and though most of them were inductive, Sanderson expects the market to grow to 700 million devices in four years. Inductive and resonant wireless chargers will ship in 2014, with resonant/bridge solutions expected to ramp up in the second half of the year.

A standard is “not taking up faster because folks are confused by the existence of what appears to be competing standards,” John Perzow, the WPC’s vice president of market development for Wireless Power Consortium, told us. “The well-known standards - Power Matters Alliance, A4Wp, WPC - those differentiating is making it hard for groups to combine... They don’t share communication protocol. They won’t talk to each other.”

But consolidation is necessary before the technology can become ubiquitous. Only inductive and radio frequency products are available to the public, with Qi inductive technology built into products such as the Samsung Galaxy S4, Nokia Lumia 920, and Google Nexus phones and tablets. Major market players such as Broadcom, HTC, and Samsung are among the members of both industry groups.

Magnetic induction currently has the wireless charging market cornered and is available in Google, Samsung, and Nokia devices. Induction typically uses two magnetic coils - a primary wire coil with an alternating electromagnetic field from within a charging base station, and a secondary coil in the device to convert power from the electromagnetic field to electrical current to charge a battery. Together, the coils create a transformer.

“If you design it right - the right frequency and material, the quality of that coil - you can get very efficient power transfer and design for specific distance or power,” Perzow said.

Several companies have taken to inductive charging. Samsung’s Galaxy S4 supports Qi, as has Google and Nokia. Perzow said the WPC has more than 40 million wireless devices on the market and has support from the semiconductor industry, Ike, and Verizon.

The WPC offers close coil inductive technology, which draws up to five Watts and operate at 200-300 kHz. Perzow said the WPC’s Qi technology can extend the charging range up to 40 mm away from the power source with 70% power efficiency.

Qi and inductive charging have been touted for having protected connections, being safe enough for medical devices, and harboring low radio frequency interference. However, inductive charging is accused of being more delicate and more inconvenient than other types of charging; users have little freedom and must line up a device precisely with a wireless charging pad.

“I think there’s something to that, but the assumption is that Qi is close couple inductive, and it will be that way forever, and that’s not the case,” Perzow said. “It is a constantly evolving technology. Qi is not a product. You can’t spec it.”

Though the WPC and Qi are currently synonymous with inductive charging, the WPC also demonstrated resonant technology at the 2014 International CES. Dubbed WoWz, the technology is backward compatible with Qi and charges at a distance of up to 18 mm with 65% charging efficiency.

“Samsung has Qi phones out there today and is also an investor in a company that is developing resonance technology that is in WPC,” Perzow said. “It’s reasonable to guess that Samsung will have resonance technology in their phones.” A WPC member and phone maker will debut a PMA+Qi compatible wireless charging system in 2014. He expects more bridge products in the coming years. “For a short term, it can work, but as soon as one standard can develop significantly, it’s going to be impossible for that approach to work.”

MediaTek, a member of WPC and PMA (now in partnership with the A4WP) debuted its own wireless charging technology at the CES - a dual-mode charging solution that supports Qi.
and resonance. The system is a stand that can hold and charge the equivalent of two smartphones. It’s built over a single coil and single IC, with a target segment of mobile applications in the range of 1/2 Watt to 15 Watts.

“The device is smart enough to figure out which charger it is, and then it charges appropriately. [The technology] goes into virtually anything you want from a Bluetooth headset to an electric vehicle,” Mark Estabrook, director of strategic marketing at MediaTek, told us. “This is something of a bridge product, we think, meaning we think it will help get the industry from where it is today - the inductive - to the resonant technology which will be developed over the next 2-3 years.”

Mark Hunsicker, senior director of product management at Qualcomm and a treasurer for the A4WP, said there is an opportunity for a dual-mode bridge transitional receiver that implements inductive and resonance charging. There’s not much legacy product in the marketplace.

Nevertheless, “I’m not a big fan,” Hunsicker said. “It’s not a highly desirable solution from the consumer side, because there’s not a great deal of commonality between the two technologies. There are increased materials and area costs, because there’s not a lot of synergy between the two technologies.”

Mohit Bhushan, US marketing manager at MediaTek, told us his company is working on resonance solutions to complement future generations of its recently released LTE SoC.

“The industry tends to use ‘inductive’ and ‘resonant’ as different technologies, though in reality, both are based on inductive technology,” Sanderson said via email. “Those which use magnetic resonance are just a highly tuned inductive solution.”

Resonant transfer relies on loosely coupled coils that transfer electricity along the same resonant frequency. A capacitance plate, which can hold a charge, attaches to each end of the coil and then produces a resonant frequency from the inductance of the coil and the capacitance of the plates.

Resonance advocates have championed the technology for the ability to charge multiple devices at once with freedom of placement - the device can be more than 10 inches above or to the side of the charging plate. Distance can also be increased by placing a repeater between the device and charging place. The A4WP says resonance (or, its version, Rezence) can charge devices through surfaces 40 to 50mm thick.

“A resonance-based approach gives the opportunity to have multiple devices charging and multiple device types. Competing forums can do some of that, but can’t meet all the requirements,” Hunsicker said. “I think you’re seeing the acknowledgement of that, because those other forums have launched resonant working groups. They’ve acknowledged that the resonant-based approach is going to overtake inductive.”

The A4WP seems best aligned to lead this charge. Its member companies include Samsung, Texas Instruments, Dell, and WiTricity, whose resonance technology IP have been used in Intel products. The group recently announced a partnership with a former inductive group, the Power Matters Alliance.
null
as those commonly found in WSNs that necessitate the use of power conversion ICs, which deal in very low levels of power and current. These can be 10s of microwatts and nanoamps of current, respectively.

An energy harvesting WSN
There is plenty of ambient energy in the world around us and the conventional approach for energy harvesting has been through solar panels and wind generators. However, new harvesting tools allow us to produce electrical energy from a wide variety of ambient sources. Furthermore, it is not the energy conversion efficiency of the circuits that is important, but more the amount of “average harvested” energy that is available to power it. For instance, thermoelectric generators convert heat to electricity, Piezo elements convert mechanical vibration, photovoltaics convert sunlight (or any photon source) and galvanics convert energy from moisture. This makes it possible to power remote sensors, or to charge a storage device such as a capacitor or thin film battery, so that a microprocessor or transmitter can be powered from a remote location without a local power source.

In general terms, the necessary IC performance characteristics needed for inclusion and use in the alternative energy market include low standby quiescent currents, typically less than 6µA and as low as 450nA. The chip should also have low start-up voltages, as low as 20mV, a high input voltage capability up to 34V continuous and 40V transients. But it should also handle AC inputs, feature multiple output capability and autonomous system power management, and auto-polarity operation.

WSNs are basically a self-contained system consisting of some kind of transducer to convert the ambient energy source into an electrical signal, usually followed by a DC/DC converter and manager to supply the downstream electronics with the right voltage level and current. The downstream electronics consist of a micro-controller, a sensor and a transceiver. When trying to implement WSNs, a good question to consider is: how much power do I need to operate it? Conceptually this would seem fairly straightforward; however, in reality it is a little more difficult due to a number of factors. For instance,

<table>
<thead>
<tr>
<th>Energy Source</th>
<th>Typical Energy Level Produced</th>
<th>Typical Application</th>
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<tr>
<td>Small solar panels</td>
<td>100s of mW/cm² (Direct Sunlight)</td>
<td>Handheld electronic devices</td>
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<tr>
<td>Small solar panels</td>
<td>100s of µW/cm² (Indirect Sunlight)</td>
<td>Handheld electronic devices</td>
</tr>
<tr>
<td>Seebeck devices (which convert heat energy into electrical energy)</td>
<td>10s of µW/cm² (Body heat)</td>
<td>Remote wireless sensors</td>
</tr>
<tr>
<td>Seebeck devices continued</td>
<td>10s of µW/cm² (Furnace exhaust stack)</td>
<td>Remote wireless actuators</td>
</tr>
<tr>
<td>Piezoelectric devices (which produce energy by either compression or deflection of the device)</td>
<td>100s of µW/cm²</td>
<td>Handheld electronic devices or remote wireless actuators</td>
</tr>
<tr>
<td>RF energy from an antenna</td>
<td>100s of µW/cm²</td>
<td>Remote wireless sensors</td>
</tr>
</tbody>
</table>

Table 1: Energy sources and the amount of energy they can produce.

how frequently does a reading need to be taken? Or, more importantly, how large will the data packet be and how far does it need to be transmitted? This is due to the transceiver consuming approximately 50% of the energy used by the system for a single sensor reading. Several factors affect the power consumption characteristics of an energy harvesting system of WSN.

Of course, the energy provided by the energy harvesting source depends on how long the source is in operation. Therefore, the primary metric for comparison of scavenged sources is power density, not energy density. Energy harvesting is generally subject to low, variable and unpredictable levels of available power so a hybrid structure that interfaces to the harvester and a secondary power reservoir is often used. The harvester, because of its unlimited energy supply and deficiency in power, is the energy source of the system. The secondary power reservoir, either a battery or a capacitor, yields higher output power but stores less energy, supplying power when required but otherwise regularly receiving charge from the harvester. Thus, in situations when there is no ambient energy from which to harvest power, the secondary power reservoir must be used to power the WSN. Of course, from a system designer’s
must be able to deal with these low power levels. While this is clear that WSNs have very low levels of energy available. Produced from different energy sources. Transducer. Table 1 illustrates the amount of energy that can be stored in the secondary reservoir when it is not available for some specified period? Is enough ambient energy available to act as both the primary energy source and have sufficient energy left over to charge up a secondary reservoir when it is not available for some specified period? Ambient energy sources include light, heat differentials, vibrating beams, transmitted RF signals, or just about any other source that can produce an electrical charge through a transducer. Table 1 illustrates the amount of energy that can be produced from different energy sources.

A nanopower IC solution

It is clear that WSNs have very low levels of energy available. This, in turn, means that the components used in the system must be able to deal with these low power levels. While this has already been attained with the transceivers and microcontrollers, on the power conversion side of the equation, there has been a void. However, Linear Technology introduced its LTC3388-1/-3 to specifically address this requirement. The LTC3388-1/-3 is a 20V input capable synchronous buck converter than can deliver up to 50mA of continuous output current from a 3mm x 3mm (or MSOP10-E) package – see figure 1. It operates from an input voltage range of 2.7V to 20V, making it ideal for a wide range of energy harvesting and battery-powered applications including “keep-alive” and industrial control power. The chip uses hysteretic synchronous rectification to optimize efficiency over a wide range of load currents. It can offer over 90% efficiency for loads ranging from 15uA to 50mA and only requires 400nA of quiescent current, enabling it to provide extended battery life. The combination of its 3x3mm DFN package (or MSOP-10) and only five external components offers a very simple and compact solution footprint for a wide array of low power applications.

The LTC3388-1/-3 incorporates an accurate undervoltage lock-out (ULVO) feature to disable the converter when the input voltage drops below 2.3V, reducing quiescent current to only 400nA. Once in regulation (at no load), the LTC3388-1/-3 enters a sleep mode to minimize quiescent current to only 720nA. The buck converter then turns on and off as needed to maintain output regulation. An additional standby mode disables switching while the output is in regulation for short duration loads, such as wireless modems, which require low ripple.

Even though portable applications and energy harvesting systems have a broad range of power levels for their correct operation, from microwatts to greater than 1W, there are many power conversion ICs available for selection by the system designer. However, it is at the lower end of the power range, where nanoamps of currents need to be converted where the choice becomes limited.

Battery management IC is first to comply to MIPI BIF

Infineon Technologies has developed the ORIGA 3 Battery Management IC to protect smartphone and tablet computer users from unpleasant surprises. The device’s proprietary PrediGauge technology enables accurate fuel gauging. ORIGA 3’s PrediGauge technology accurately determines remaining battery capacity under the most adverse conditions. Within a few minutes of battery relaxation the IC predicts the future OCV and therefore the charging state within an average accuracy range of one percent. Additional functions of ORIGA 3 comprise precise temperature sensing as well as inputs for several sensors such as external temperature, strain gauge, and humidity. All information gathered by the IC is transferred to the host device (smartphone or tablet) using the MIPI BIF digital protocol. The hardware authentication feature of ORIGA 3 helps to identify unauthorized batteries. The ORIGA 3 authentication is based on an enhanced version of elliptic curve cryptography (ECC). The ORIGA Digital Certificate feature allows individual keys for each chip. It also enables secure field updates of the firmware.

Infineon Technologies

www.infineon.com

Rapid charge controller supports MediaTek fast charge protocol

Dialog Semiconductor plc has unveiled the world’s first AC/DC rapid charge controller compatible with MediaTek’s new Pump Express fast charge protocol which claims to enable rapid charging of mobile devices up to 45 percent faster than conventional chargers. Dialog’s IW1680 is a single-chip solution that reduces charge times in USB AC/DC wall chargers with no bill of materials (BOM) cost premium compared with slower conventional charging technologies. The IW1680 uses Dialog’s built-in, intelligent rapid charge digital algorithm that communicates with MediaTek Pump Express-compatible phones and dynamically scales the output voltage of the wall charger to deliver the optimized level required by the phone at any given time. The overall system cost is lowered by eliminating the need for an input buck converter in the phone and reduces charge times by enabling more efficient power transfer to the phone battery. The IW1680 rapid charge AC/DC controller embeds digital analysis on the primary side of the isolated power supply within the charger, supporting voltage scaling without the need for any intelligence on the secondary side.

Dialog Semiconductor

www.dialog-semiconductor.com
AFEs integrate up to eight 24-bit ADCs for multiple load power monitoring

The MCP3913 and MCP3914 energy-measurement analog front ends (AFEs) from Microchip Technology integrate six and eight 24-bit, delta-sigma Analog-to-Digital Converters (ADCs), respectively, with 94.5 dB SINAD, -106.5 dB THD and 112 dB SFDR for high-accuracy signal acquisition. The MCP3914’s two extra ADCs enable the monitoring of more sensors with one chip, lowering cost and size. Additionally, the programmable data rate of up to 125 kspS with low-power modes allows designers to scale down for better power consumption or to use higher data rates for advanced signal analysis, such as calculating harmonic content. These AFEs also feature a CRC-16 checksum and register-map lock, for increased robustness. The company also announced two new evaluation boards to aid in the development of energy systems using these AFEs. Both chips come in 40-pin uQFN packages, the MCP3913 adds a 28-pin SSOP package option.

Microchip
www.microchip.com

2.5A and 4A gate drive optocouplers boost power efficiency

Avago Technologies’ latest gate drive optocoupler devices, the ACPL-336J and ACPL-337J, offer a 2.5A and a 4A rail-to-rail output, respectively, capable of driving high power MOSFET or IGBT directly. The devices feature rail-to-rail output with high current, integrated LED driver, active Miller clamp, high DESAT blanking current source, and Under Voltage Lock-Out (ULVO) feedback control circuit, providing a complete cost-effective gate drive solution for motor control and power inverter applications. The chips come with a wide creepage and clearance of 8.3 mm meeting stringent system level safety regulation. They have 50kV/µs typical high CMR preventing erroneous drive in noisy environment.

Avago Technologies
www.avagotech.com

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Model-based design of multi-physics automotive systems

By Sujit S. Phatak and DJ McCune

TODAY’S VEHICLES epitomize the concept of multi-physics systems. Design teams are bringing together software and electronics, along with airflow and environmental sensors, mechatronic, hydraulic and pneumatic subsystems, to create increasingly sophisticated automotive systems.

Traditionally, the automotive industry has made extensive use of “downstream” engineering. Design teams have followed the traditional “V-cycle”, which splits the engineering process into two phases — design and implementation followed by validation.

While design teams can benefit significantly from earlier validation of their concepts, the industry has historically favored physical prototyping as a means of validating the design, which requires a commitment to build a hardware prototype early in the project lifecycle.

This is often followed by a sequence of reworking, patching and more prototyping. Design teams pursue this cycle until the design appears to be bug-free. Unfortunately, such a downstream approach to engineering can lead to periods of prolonged patch fixing while engineers chase their tails and lose production cycles. If we cannot fix the design by patching, it may require a complete re-design. In the worst case, we may not discover the problem until the vehicle is in production, which can lead to disastrous product recalls.

Upfront engineering

While simulation doesn’t remove the need for physical prototyping, it does considerably reduce the number of prototyping cycles that we need to go through during a project. By spending more time upfront with the design, we avoid many of the downstream problems.

Simulation enables us to learn more about the system and understand how it works. Because simulation models give us better visibility into the way our designs work conceptually, we can get rid of bugs — hopefully before we build them into the prototype. An additional benefit is the ability for new team members to get up to speed with the design by experimenting with the simulation, which doesn’t risk causing damage to (expensive) physical prototypes.

Cyber-physical systems

A model-based cyber-physical systems (CPSs) development approach as shown in figure 1 enables design teams to integrate physical processes with computational systems during simulation. These virtual CPSs support abstractions appropriate for modeling and design, and analysis techniques suitable for integrated systems.

The mechatronic control systems that are implemented in automotive applications include those used for engine control, transmission control, throttle control and braking. These typically involve multiple complex physical systems with dedicated embedded controllers that communicate with each other via a vehicle network, such as Controller Area Network (CAN) or FlexRay.

We have adopted model-based design for CPSs to improve the efficiency of the design process for these complex systems. During the system design stage we integrate models of physical system behavior (also called “plant models”) with controller models to produce an abstracted system implementation.

Accelerating project schedules

Simulation enables us to fix bugs before they manifest themselves as problems. That can sometimes make it difficult to put a value on our use of simulation in terms of the engineering time saved or improved design quality.

However, a typical prototyping cycle might take us approximately six months. By introducing a model-based CPS, we can reduce that to around two months by breaking the “prototype/bug-fix” cycle. For derivative projects, we will typically go through two or more prototyping spins to accommodate new requirements, while updating the simulation models will often only take a couple of days.

We are also interested in the use of model-based design for more experimental work. For example, we are considering the use of multicore devices for our next-generation advanced architectures, which we don’t use in our products today. Simu-
loration will enable us to investigate and optimize these new architectures before we spend time implementing them.

Using the right tool for the Job
We use a portfolio of simulation tools to suit the task in hand. For mathematical modeling of signal flow or behavior we use MATLAB/Simulink. For modeling hydraulics systems we use AMEsim. As soon as we get away from modeling control algorithms and into the electronics domain, then Saber is our tool of choice. Saber supports the concept of conserved system modeling, which allows us to analyze the effects of how one block loads another — something that’s not possible using a signal-flow analysis. Saber also allows us to model events and event transfers, whereas SPICE simulation, for example, uses the continuous (Laplace) domain.

Case study: modeling a gasoline pump
The physical system of a gasoline fuel pump as shown in figure 2 consists of three parts: a driver circuit simulated using an electromechanical simulator, and separate pump and inlet valve models, which are simulated using the hydraulics simulator.

To create the multi-domain simulation shown in figure 2 we used Simulink to model the control part of the ECU algorithm and deployed a combination of Saber (simulating the hydraulics of the fuel pump) to model the plant.

It’s a common misconception that Saber is only useful for modeling a system’s power electronics; it actually does a very good job of modeling the electromechanical parts of the system. For example, by getting accurate readings of the force from the electromagnetic circuitry for a solenoid, we can use it to send out a force and receive back a position.

We used proportional-integral (PI) control to generate the controller output based on the difference between the target pressure and the pressure feedback at a constant battery voltage input level. Triggering the solenoid in response to the controller output uses energy, so we added pulse width modulation (PWM) duty-cycle control to the original control. While the solenoid had to be fully triggered to open the inlet valve, less force was required for holding it open and therefore we could reduce the current through the solenoid. The percentage reduction in the solenoid current was determined by the PWM duty factor.

Following several tests and using our experience, we gathered data on the relationship between the duty factor for various start angles and the revolutions per minute (RPM) and battery voltage. We then produced a look-up table that could be used to obtain the duty-cycle value. The PWM-based control also enabled the use of the virtual CPU based approach for implementing this CPS.

We also use Saber to analyze the first-order hysteresis effects of magnetic circuits—see figure 3. This is much simpler and less time consuming than performing a finite element analysis, which has its place if you need to look at fringe effects, but otherwise Saber gives us the right level of detail for system modeling without too much complexity.

The future of modeling
Given our globally distributed teams, we’re very interested in the emergence of cloud computing to harness global CPU resources and enable us to share higher fidelity models across distributed teams. Today, we are using the cloud to deploy product lifetime management (PLM) applications, but with an increased use of simulation and co-simulation over the next 10 years we can see our use of the cloud transitioning from a manager’s tool to an engineer’s tool.

Increasingly, we are encouraging the use of virtual CPU modeling, which involves developing a software model of the microcontroller hardware itself. We can then integrate the microcontroller model with the behavioral models of the plant (the physical system) so that we can perform realistic system performance measurement and validation. This approach allows concurrent development of the plant models and control software applications, and also their validation, including the real-time operating system (RTOS) and device drivers.
Eight tips to accelerate SoC physical design at RTL

By Francois Rémond

The growing complexity of modern System on Chip (SoC), the design effort associated with the increasing pressure on silicon cost, and the pressure associated with shortened schedule requirements, makes it essential to use innovative implementation approaches to optimize silicon area and ensure a short and predictable timeline.

Silicon design usually suffers from the disconnection of needs between logical designers and physical architectures. This disconnect leads to costly iteration loops to reconcile incompatible options taken by design teams working in isolation. In this article, we will review the essential points to consider in order to ensure a smooth transition between the logical and physical worlds.

Logical and physical implementation context

Let's have a look at the situation. At the beginning of the design process, the SoC's initial representation is captured based on the functional description of the circuit and the logical architecture suitable to achieve the functionality and performance. This is usually expressed as shown in figure 1.

When it comes to physical implementation – with the assumption that flattening the entire design is not an option due to the size of modern SoCs and the limited capacity of place and route tools at deep submicron nodes – we have to determine a suitable hierarchy for the backend implementation to result in an optimal design.

The traditional approach was to mimic, in the physical domain, the hierarchy inherited from the RTL coming from the logical assembly of the SoC – see figure 2a. The main drawbacks with this approach are the huge complexity of the top-level floor plan, the overall synchronization of the sub-block’s development and the final timing convergence.

Recently, it became more common to harden some specific parts of the design, creating the adequate level of hierarchy in the RTL and flattening the remaining part of the SoC – see figure 2b. The benefit of this methodology is that it limits the complexity of the top-level floor plan. However, since the bus fabric is implemented at the top level, timing convergence remains a challenge, and the wire dominant nature of the bus potentially makes the silicon utilization less than optimal.

To further improve the previous approach, a designer can choose not to have any logic at the top level of the circuit by pushing all the circuit components, including bus fabric, within the physical partitions leaving only inter-partition connections at top level – see figure 2c. The designer could alternately connect those physical partitions by abutment (inserting feedthroughs for the connections having to traverse a physical partition). This approach leads to an extremely optimized usage of the silicon (as the wire dominant nature of the bus is merged within blocks which are more gate intensive), along with a predictable timing closure, provided a number of good design practices have been followed.

Looking at figure 2c, it is obvious that the physical hierarchy is not reflecting the functional hierarchy that was elaborated during the logical assembly of the SoC in figure 2a. Let’s investigate how to move from the logical to the physical domains.

Tips for optimized SoC realization

At the beginning of the implementation process, it is important to identify the degrees of freedom that exist: The IO ring (typically predefined) provides strong constraints to the placement of interface blocks, while the elements that primarily connect to the internal bus have more flexibility for their location within the die.

Balancing the physical partition area

If at all possible, having physical partitions of similar size simplifies the top level floor plan along with the pin distribution at the partition border. Accommodating blocks of extremely different sizes often requires creating complex rectilinear shapes leading to a more congested routing.

Minimizing top level routing

Reducing the number of wires to be routed at top level (or using

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www.atrenta.com
feedthroughs) is a good design practice to make the top level more easily implementable. In order to achieve the target, cloning of specific logic blocks which generate many distributed wires across the die (like reset and DFT controllers, or some clock generators) will help.

Minimizing high speed connections
If the connections between physical partitions can be low-speed connections, the final timing convergence will be easier. Clever IP grouping choices will help achieve this goal.

Optimizing the clock distribution
Enforcing “clock confinement” (i.e. having synchronous clock domains bounded inside a single physical partition, as opposed to an SoC-wide distribution of synchronous clock) is the best strategy along with minimizing high speed connections to ease the top level timing convergence. If properly achieved, along with reasonable timing budgeting at the physical partition border, it will allow confining the timing challenges within physical partitions (and then solving them locally). As a result, the final assembly of the SoC will not exhibit problems requiring reopening already timing clean partitions.

Honoring power domains
Multiplication of independent power domains (either standby area or DVFS domains) in circuits for the mobile market creates additional constraints to honor when defining the physical implementation strategy. Special care must be taken to ensure that different power domains will be properly isolated and that feedthrough signals (which can possibly cross power domain boundaries) will be buffered on the proper power supply.

Optimizing the bus fabric architecture
All the techniques listed above will drive the design team to rethink the bus fabric architecture according to the physical implementation needs. Doing this will allow the design team to match bandwidth and latency requirements and take each of the previous points into account during the final optimization of the bus design.

Physically driven grouping of IPs has major implications on the bus architecture which cannot be anticipated at the early design stage. For a given class of traffic, permutations of IP connection slots will be done to allow the proper IP grouping to take place. And the timing optimization of the bus design (pipeline insertion) cannot be done before this final version of the bus being available.

Verification of clock and power domain crossing
A single clock domain crossing error can kill the functionality of the entire SoC, by introducing non-deterministic flip-flop metastability behavior. This leads to random failures depend-
ing on PVT conditions which are extremely costly to debug at silicon level. This verification can’t be delayed until the final SoC assembly but needs to occur in a hierarchical way; it must be an intrinsic part of the design process. Special care must be taken as the context of integration of an IP may change the clock relationships with respect to the original IP designer assumptions. All asynchronism/synchronism assumptions have to be carefully reviewed. It is also important to eliminate synchronism assumptions between different power domains as those are almost impossible to close across the variety of possible voltage scenarios.

Completeness of timing constraints
The quality of the timing constraints that will be used to signoff the design is another key item to watch. The creation of the final SoC level SDC is a combination of a bottom up and top down approach. Timing exceptions are inherited from the IP, and clock constraints are propagated from the top of the SoC. Insuring the coherency between the various sets of SDCs is not a trivial task, especially when design is built from multiple sources (3rd party IPs, internal design reuse, new design blocks, etc...) and the team is located on different continents (which is the case for most modern designs). Here, communication between the team members is the challenge.

Those timing constraints have to be validated early in the design process for all modes of operation to drive the physical implementation. If properly budgeted at the border of each physical partition (and signed off at the partition level after implementation), then the final assembly and chip timing closure will not be a major challenge.

Restructuring the design RTL
We discussed the benefit of restructuring the design hierarchy to fit with optimized implementation.

The question now is: at which stage of the design should this restructuring occur? There are two main reasons to restructure at the RTL:

Benefit from RTL synthesis at physical partition level
a) Propagating the input tie-up, tie-down, and floating outputs though the hierarchy will reduce the size of the netlist to implement. This reduction comes for free during the synthesis process, while it is more complex to implement at the netlist level where scanned flip-flops prevent this optimization to occur within a stitched scan chain.
b) In-context synthesis with wire load models estimated from the predicted size of the physical partition will produce an “easier to implement” netlist with respect to timing criteria.
c) Physically-aware DFT insertion (scan ordering and compressor insertion) will reduce congestion spots.

The enabler for RTL restructuring to occur is the starting of high-level design floor planning and timing evaluation from the RTL representation. There are now reliable tools on the market to perform this task with adequate precision, in order to generate the directives for the RTL & SDC manipulation to happen. The sequence of operations is depicted in figure 3.

To better control schedule predictability
Starting this physical activity at the RTL is another way to discover early on (at a time where the RTL design may still be influenced), blocking points that could end up in long fixing iterations if discovered at the final stages of the design closure. This is called “prototyping.” A coarse grain synthesis followed by a fast placement generates a representation of the whole SoC which is used to evaluate congestion and timing issues early on, and determine corrective actions. It is the starting point of the partitioning activity we discussed above.

The benefit here is to eliminate the loops from final timing analysis to RTL design, replacing them with local loops that are easier to control.

The case study highlighted below shows the advantage of allocating time for “prototyping” the physical implementation of the whole SoC in advance (scenario 2 and 3 compared to scenario 1 in figure 4) along with the additional benefit of doing this prototyping at the RTL rather than at the netlist level (scenario 3 compared to scenario 2).

Design complexity and market pressures make the die area and schedule control of modern SoCs important success criteria. It is therefore crucial to anticipate and validate critical design decisions as soon as possible. It is now possible to do this assessment at the RTL to bring more physical awareness within the RTL design phase to further optimize the silicon utilization and bring more controllability in the implementation process.
Embedding components within PCB substrates

By Max Clemons

Embedding components within a PCB substrate offers a range of benefits in terms of space and performance. But this alternative approach to product design demands support from the entire supply chain, including EDA vendors.

Continued pressure for electronic devices that provide greater functionality in ever-smaller form-factors is not only providing the driving force behind developing smaller surface-mount components and semiconductor geometries, but is also fuelling another trend that sees passive and active components being embedded within PCB substrates.

It is a trend that has a significant impact on the entire electronics supply chain, a challenge that suppliers at every stage are now striving to meet. Making best use of these developments falls to the design engineering team, who now need access to design automation tools that can offer greater flexibility in the way PCBs are conceived and created. The design rules of this new paradigm present their own challenges and it is here where EDA tools vendors are now focusing their development efforts, in order to enable more OEMs to gain competitive access to this enabling and evolutionary capability.

Components

There are essentially two methods for embedding components into a substrate: formed or inserted. The former effectively uses patterns of copper plating and resistive thin film to create passive (resistive, capacitive or inductive) components on an embedded (or surface) layer. The latter is the more evolutionary, as it allows discrete components, bare die or even modules to be placed below the surface of the substrate.

There are many benefits to this and perhaps most prevalent is the greater component density it offers. An important aspect of this is the increased need for passive components, particularly capacitors which are needed in direct response to higher operating and signal frequencies. This has given rise to a trend to stack components vertically in order to minimise track lengths. Texas Instruments recently brought a 500mA step-down DC-DC converter to market using this method, to create a module measuring just 2.3mm by 2.0mm and just 1.0mm high.

Component manufacturers must constantly meet demand for new packaging options when bringing products to market, and the widespread use of surface-mount technology (SMT) — particularly in passive components — lends itself well to embedding components into PCBs. As SMT profiles continue to shrink, these same parts can now be mounted within or directly alongside a die embedded within a PCB; the 01005 (0402) package, for example, measures just 0.4mm by 0.2mm and can be as little as 0.15mm high.

However the method used to provide connectivity introduces further requirements. There are essentially two options here; connections formed with traditional soldering, or using copper vias.

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When solder is used, general-purpose tin plated multilayer ceramic capacitors can be used, but this comes with a risk when embedding; secondary heating (when mounting SMTs on the surface, for example) can cause the solder paste to reflow around the embedded component and introduce possible failure.

To overcome this, the industry is beginning to displace soldering embedded components with connectivity through copper vias, but while this scenario avoids the issue of solder reflow, the components’ electrodes also need to be copper (as opposed to tin) in order to guarantee good connectivity. As a result, the industry is now producing SMT devices with copper electrodes, such as the GRU series introduced by Murata, which are intended specifically for embedding.

Manufacturing

In a traditional workflow, the manufacturing stages are often discrete; the bare board is fabricated before being passed to assembly, where component placement machines are used to populate the PCB. In the embedded component paradigm this changes; these stages are no longer discrete, as components now need to be placed within the PCB while it’s being fabricated. This presents challenges for both the PCB industry and the manufacturers of production equipment.

Components that are embedded within the substrate are placed within a cavity, either during or after the PCB substrate is fully formed; if the component can be placed after the PCB is complete the cavity is typically open on the surface. If the component is encapsulated within a multilayer board, the component is completely embedded and must, therefore, be placed by the PCB manufacturer, which is creating a new market opportunity for SMT placement machine manufacturers.

Correspondingly, SMT machine manufacturers must also now consider the demands of embedded component placement. Often the cavity will offer very tight tolerances, perhaps as little as 20μm, which creates a need for greater accuracy with SMT placement. For example, the self-alignment effect of solder paste can overcome a level of inaccuracy, but this is not the case with embedded components.

In addition, the force with which components are placed needs to be more closely controlled; damage to surface-mounted SMT components caused during placement can be found through visual inspection, but embedded components are typically not visible and so any fractures incurred could render an entire board faulty. Additional thermal events, such as reflow soldering on surface-mount components, can also compromise the integrity of embedded components.

Suppliers of manufacturing equipment are now fully involved with the standards and best practices emerging to ensure embedded components will continue to benefit the industry at both a functional and commercial level.

EDA Tools

The electronics industry has successfully adopted the concept of embedded active components to the point where it is becoming mainstream. Although pioneered by large-volume OEMs targeting consumer devices, where every square millimetre is valuable real estate, support for smaller design teams has increased in recent times, enabling OEMs of all sizes to exploit the benefits of embedded components.

This support comes predominantly from EDA vendors; the latest release of Altium Designer (Version 14), for example, introduces advanced features for defining and implementing cavities in PCBs to support embedded components.

More PCB fabrication flows can now accommodate embedded components through cutouts and laser drilling, as shown in figure 1. In order to exploit this capability, Altium Designer 14 (AD14) supports a Region attribute called Cavity Definition, which associates a Height to regions, and allows components to be placed on any signal layer. As well as being completely embedded, a component’s cavity may also extend to the edge of the PCB and therefore be open on one side. This can be particularly useful for embedding SMT LEDs in a board, for example. Figure 2 shows a cavity for an SMT LED in a round PCB, designed using AD14.

By editing a component’s properties, the layer can be defined as any internal layer, while the orientation of the embedded component will be defined by the orientation for that layer (although this can be overridden by enabling the Flipped on Layer checkbox). When a component is embedded in this way, Altium Designer 14 automatically creates a Managed Stack, which defines the board structure in the Z plane. There are now several methods for embedding active components open to developers:

- Integrated Module Board (IMB); Embedded Wafer Level Package (EWLP); Embedded Chip Build Up (ECBU), and Chip in Polymer (CIP). The last process allows thin wafer packages to be integrated directly into build-up dielectric layers, rather than using cavities drilled or routed into the core material, which also supports multilayer FR-4.

An important aspect to ensuring success when designing with embedded components includes communicating effectively with the PCB fabricator, and Table 1 outlines the recommended documentation that should be provided to the PCB fabricator, along with the design files.

While embedded components have been used for around 10 years by large OEMs in high-volume consumer applications, their availability and support is increasing throughout the electronics supply chain. This, in turn, is creating new opportunities for OEMs of all sizes, targeting a range of vertical markets, who can now exploit their advantages.

Design engineers represent the interface to this supply chain, and EDA vendors provide the tools to make that interface as seamless and effective as possible. Through adding greater support for designing PCBs using embedded components, Altium continues to enable effective electronic product design at every level.

Table 1: Recommended documentation that should be provided to the PCB fabricator.

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|---------------------------------|---------------------------------|
| Layer Stack Diagram | Cursory diagram showing the location and orientation of cavities for embedded components. |
| NC Drill File | Separate file should be generated to account for cavities. This information is much more detailed and accurate than a layer Stack Diagram, and will be used during bare-board fabrication for routing or punching. |
| Fabrication Notes | Any useful information for the fabrication process should be noted. This may include specific substrate material choices, or polymer and epoxy materials used to fill cavities. |
| Pick and Place File | Separate file should be generated for components to be embedded. Information about component locations, rotation, and layer is contained within the file. |
| Assembly Notes | Additional assembly information not included in the Pick and Place file should be noted. This may include whether the component is flipped on the layer, or any special assembly instructions. |

Fig. 2: Designing a cavity for an SMT LED in a round PCB.
DDDR4 PHY IP reaches 2667Mbps at 28nm: 3200Mbps next?

Cadence Design Systems claims it has achieved 2667 Mbps performance on its double data rate fourth generation (DDR4) PHY Intellectual Property for 28nm, an industry’s best according to the EDA vendor. By providing both the DDR4 controller and the DDR4 PHY at that high speed, the company will allow designers to truly leverage DDR4 high-speed memories into servers, networking and consumer applications. “In 28nm, there has been no DDR4 IP in the market that we are aware that has achieved any more than 2400Mbps”, commented Andrea Huse, Senior Marketing Manager at Cadence Design Systems. “In general, IP for DDR3 has been in the 2133 Mbps range on the high side and we are currently planning DDR4 – 3200 IP using a smaller geometry node” she added. The DDR4 PHY IP will support higher densities than DDR3, but it has other significant advantages over DDR3, including greater reliability, better power efficiency operating from 1.2V instead of 1.5V for DDR3, higher capacity, explained the EDA vendor. Reliability, availability, and serviceability (RAS) are more robust since DDR4 supports command and address parity error detection and recovery, command blocking upon detection of parity error, but also a connectivity test mode. DDR4 also provides optional features like CRC protection for write data.

Cadence
www.cadence.com

EDA tool verifies design rule check decks

Sage Design Automation’ DRVerify is a new tool that verifies design rule check (DRC) decks. Used by process design kit (PDK) teams and DRC deck developers, DRVerify addresses the problem of DRC deck errors, especially in leading edge process nodes of 20nm and below. DRC deck errors that are found late in the design or after tapeout are very costly, and can cause yield issues, incur additional redesign and mask costs, and ultimately hinder the production schedule. Using the design rule definition as input, DRVerify generates an exhaustive set of tests that thoroughly checks the correctness and accuracy of the DRC code as it is being developed. New advanced semiconductor process technologies, at 20nm and lower, come with new design rules that are extremely complex. Implementing DRC checks for such rules is a laborious and error-prone manual programming task, and thus the resulting code can easily have errors and inaccuracies. CAD teams and designers try to create sets of layout test cases exhibiting both “pass” and “fail” conditions and use them to check the DRC deck. Today these tests are usually devised and made manually or assisted by scripts or layout design tools. DRVerify uses the iDRM formal graphical rule definition as its input, and generates test cases based on that input. It systematically searches all boundary conditions of the rule expression and creates every possible variation of the design rule expression that can change the check result. Using a sophisticated layout engine, DRVerify generates thousands of test cases per rule in a matter of minutes. In addition to verifying DRC decks, DRVerify is also used by design rule manual (DRM) teams to validate DRM design rule specifications.

Sage Design Automation
www.sage-da.com

Optimized dataprep flow speeds up maskless lithography

In a joint program, Aselta, a supplier of advanced data preparation software solutions, and Mapper Lithography, a supplier of electron-lithography equipment, have developed an optimized data preparation flow for geometries from 90 nm down to 14 nm nodes. The challenge of advanced multi-beam writers, especially at 20nm and below, is to find the optimal trade-off between wafer pattern fidelity which drives yield and writing time which ultimately drives cost. The solution for the Mapper’s writer is based on Aselta technology, Inscale, which correction algorithms provide a unique combination, allowing customers to reduce cost while augmenting quality. The software flow features a dedicated proximity effect correction, a simulation and analysis capability and a model-based verification engine fully interfaced with the oasis.mapper format. A complete FLX:1200 emulator has been implemented in order to mimic the pixelated data handling through the full data path. Simulation inside Inscale is achievable pixel-wise with a bitmap repartition identical to the final multi-beam exposure. On top, several software modules have been implemented like rasterization and dose mitigation. A new SmartBoundary scheme is adapted to Mapper’s data format to minimize alignment and stitching errors.

Mapper Lithography
www.mapperlithography.com
Choosing the right housing materials for DDR4 memory modules

By Siang Hock Quah and Wai Kiong Poon

GREEN DESIGN IS, and will remain, the subject of significant attention in the electronics industry. Besides looking for more efficient energy consumption, OEMs are increasingly restricting the use of halogens in flame retardants in plastics used for such items as connector housings. The memory that supports next-generation Green Design must therefore meet the diverse demands of higher performance, increased power density, improved reliability, low power consumption and avoidance of substances of hazardous concern.

DDR4 is the latest type of synchronous dynamic random-access memory (SDRAM) now coming onto the market. It has higher clock frequencies and data transfer rates than DDR3, and is not backwards-compatible, due to, among other things, differences in signaling voltages and physical interface. The technology also puts higher demands on materials used to house and insulate the memory modules and sockets.

Various high performance thermoplastics may be used to injection mold socket housings for the new DDR4 generation of memory modules. Specifiers need to pay close attention to important differences in the performance of these materials, since they have critical effects on key parameters in the finished part, such as warpage, connector reliability, pin retention forces, and compatibility with the printed circuit board (PCB).

The common termination methods used for DDR4 are: Surface Mount Technology, SMT, which will be the main termination method in the future; Pin Through Hole, PTH (currently a mainstream technique, mostly applied in desktops); Pin-in-Paste (used mainly in All-In-One PCs); and Press Fit (used in Telecoms). Depending on the OEM and specifics of the board design such as the number of PCB layers, any of the above DDR4 connector types can be applied.

Differences in the details of connector designs can directly trigger the choice of the housing material. For Pin-In-Paste and SMT designs, for example, very high temperature resistant plastics are a must because they have to withstand the reflow soldering step during assembly. Here, the connector is exposed to lead-free assembly temperatures in the range of 260-280°C, with some spots reaching even higher temperatures. Connector housing materials must be able to withstand the peak temperature for around 10s. Furthermore, materials must show a proper balance of low moisture absorption and high surface tension. This avoids the formation of blisters which can appear during high IR-reflow processing temperatures.

DDR4 connector requirements

In the figure 1, the left star diagram shows the performance of materials tested for SMT DDR4 connectors intended for mounting onto the PCB using SMT. Designs require housing plastics of the highest temperature resistance and mechanical performance. Zero blistering during reflow soldering and excellent coplanarity are the two key qualifiers (Q). Insufficient performance in either of these two criteria excludes a material from use in DDR4. The diagram on the right shows data for PTH press fit designs. Somewhat less critical design parameters are the so-called differentiators (D).

The design and type of connector determines the set of materials that can be considered for the housing. For the SMT/ULP (Ultra-Low Profile) connectors, these materials are: Liquid

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Crystal Plastic (LCP); polyphthalamide (PPA) PA10T, polyamide PA4T and LCP/polyphenylensulfide (PPS) blends; for the PTH/Press fit design, these are the polyamides PA4T, PA46 and PA66 as well as PPA.

Effects of CLTE, flow and HDT on coplanarity
Warpage in a connector happens when the connector loses its co-planarity before or while being soldered onto a PCB. Such warpage is a complex phenomenon, driven by various parameters such as the heat distortion temperature (HDT) of the material used for the connector housings, a difference in the coefficient of linear thermal expansion (CLTE) between the plastic body and the PCB, and the flow properties of the housing material, which are coupled to the stress built into the housing during injection molding.

To achieve good co-planarity of the connector on the FR4 or latest halogen-free PCBs, there has to be a close match in CLTE between the board and the connector housing material. In addition, a combination of high stiffness and high heat distortion temperature (HDT) under load is required to ensure low warpage after reflow soldering. The CLTE mismatch between the FR4 board and PA4T is lower than between FR4 and LCP. The difference is even more noticeable when mismatches with the new generation of halogen-free (HF) PCBs are considered. The CLTE of an HF PCB is still closer to that of PA4T, and yet further away from LCP.

In producing good quality DDR4 connectors while keeping costs to OEMs affordable, manufacturers look for housing materials that have the highest possible flow while meeting other key design requirements such as mechanical properties or colorability. Use of a high flow material enables the use of injection molds with a high number of cavities, increasing productivity. At the same time, use of a high flow material leads to less incorporated stress in the housing. If a housing has stress built into it, that stress will cause the housing to warp when it is exposed to high temperatures during connector assembly. As a result, it is possible that signal pins at both ends of the connector will lose their electrical contact to the PCB.

Traditionally, when a molder or connector manufacturer is looking for high flowing materials, LCPs have often been the material of choice. From a simple flow perspective, LCPs show the best performance, followed by PA46 and PA4T. But while LCPs have done an acceptable job in connectors up until the DDR3 generation, from DDR4 onwards all LCPs are failing in warpage. After molding, there is little difference in warpage between connectors made in LCP and connectors made in PA4T and PA46. After assembly to the PCBs, however, LCP housings show a significant warpage, often with a change (or “flip”) in the direction of the warpage, which makes any prediction and warpage correction in the design virtually impossible. Even blends of LCPs with PPS, in which the higher stiffness of the PPS leads to some improvement in warpage, and which have been used in DDR3, do not meet the required co-planarity levels in DDR4. When the connectors are made in PA4T or PA46, however, the warpage after assembly is significantly lower and width and height, and the higher pin count of DDR4 connectors.

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well below the 0.1mm specification. Moreover, both polyamides do not show any flip in the direction of warpage.

A key indicator of warpage is the Heat Distortion Temperature, or HDT, of the used housing material. HDT defines the temperature where the polymer becomes soft and starts to deform under a specific load. Figure 2 shows the HDT-A (1.8MPa load) of various materials which have been tested for DDR4 connectors.

The yellow bar indicates the range of HDT values that is borderline for good warpage performance during the assembly process of connector assembly. Materials with an HDT below the bar cannot be used for connectors attached to the PCB with reflow soldering. Materials with an HDT inside the yellow bar are likely to require significant design and manufacturing efforts (such as mechanical fixation by clamps during assembly) in order for them to be used. Materials with an HDT above the yellow bar show low warpage even without any fixation to the board. Only PA46 and PA4T show high enough HDTs to ensure low warpage even without any fixation to the board. PA46 and PA4T have been found to be the most suitable materials for PTH and Press Fit designs. PA46 has been found best in class, keeping the required 0.3kgf/pin also after soldering. Other materials such as PPAs (PA10T, PA6T/66) or PA66 may provide sufficient force during connector assembly, but show a strong decay below the specified 0.3kgf/pin after soldering.

Conclusions

The challenging design of DDR4 and the various changes from previous DDR3 technology have significantly increased the application requirement for mechanical strength, pin retention force and flow. Due to its outstanding combination of flow and mechanics, PA46 has been found to be the most suitable material for PTH and Press Fit designs. PA46, with its approximately 25°C higher melting point combined with a higher surface tension and a lower moisture absorption, is considered the material of choice for SMT and ULP designs.

Warpage in connectors is increasing in importance with the growing trend towards SMT, ULP and VLP designs, the growing number of DDR sockets per server board, and the risk that warpage in a connector could even bend an entire PCB. Warpage combined with insufficient mechanical strength disqualify LCPs from the upcoming DDR4 technology. Legislation governing the use of hazardous materials, such as the European Union RoHS (Restriction of Hazardous Substances) Directive 2011/65/EU, is providing a further spur for the use of thermoplastics whose flame retardant properties do not depend on halogenated additives. PA46 and PA4T polyamides are available that contain neither halogens nor phosphorus-based flame retardants. They will ensure full future compatibility with customer requirements, avoiding the need for any further requalification at either the connector manufacturer or the OEM.

Fig. 2: HDT-A (1.8MPa) of various polymers. The temperature range highlighted in yellow is required in order to enable low warpage and to avoid collapse of the side walls of the connector.
The slope of the line is key to ESD protection

By Jim Colby

AS THE COMPONENTS used in high-quality electronic products, televisions for instance, continue to shrink, the circuitry becomes increasingly more sensitive and difficult to protect because of the deep sub-micron silicon processing used to create them. Transient over-voltage events can then cause soft, latent or even catastrophic failures.

Electrostatic discharge, more commonly known as an ESD event, represents a common, over-voltage transient. And, in fact, modern ICs are generally equipped with a minimum level of ESD protection to safely survive the manufacturing process. However, the level is typically very low (i.e. 500V) and the ESD test model used is nothing like what can be seen in the field while the application is in the hands of the user. As a design engineer, it is important to note that significantly higher ESD levels can be generated during day-to-day use of their product. For instance, humans can generate ESD levels in excess of 15kV simply by walking across a carpet. If an ESD event of this severity is discharged into a USB port, for example, it can severely damage on-chip protection circuits and the circuitry they are meant to protect. This would then render the USB useless.

Protection for sensitive ICs needed

A case in point illustrates how closer collaboration between global electronics manufacturers and their component supplier can be the key to developing solutions to these problems: Last year, a market-leading manufacturer of consumer electronics, mobile communications and home appliances contacted Littelfuse to help them solve a potentially serious problem. They determined that a key IC was experiencing frequent damage via the USB port. The IC in question was used to make an LCD TV “smart” by providing WiFi connectivity. The company had already tested many different devices and only been able to obtain a maximum of 3.5kV with respect to the system’s ESD immunity. None of the ESD solutions from other companies had been able to meet their requirements for protection. After investigating the design and understanding the target ESD immunity levels, Littelfuse confirmed that it could in fact provide a device capable of meeting their needs.

The two companies met at Littelfuse’s manufacturing and testing center in Wuxi, China, so they could determine an appropriate solution. During the application-level testing, Littelfuse demonstrated the importance of dynamic resistance (of the ESD suppressor) on system level performance. Dynamic resistance is the effective resistance of the suppressor while clamping an ESD pulse. This is the key factor in determining how well a device will shunt the ESD pulse which ultimately determines if the IC will be protected or not. Another way to look at this is that the V-I curve of the protection device will have a gentler slope with lower dynamic resistance. By testing a multitude of off the shelf devices with varying dynamic resistances, it was determined that a device with a dynamic resistance of approximately 0.25Ω (measured via TLP or Transmission Line Pulsing) would protect the IC sufficiently. Ultimately Littelfuse confirmed it could design a new device in the desired form factor with a dynamic resistance very close to what was needed, and still keep the capacitance sufficiently low to preserve signal integrity of the USB port.

The SP3031 was born

Four months later, we had successfully provided the SP3031-01ETG, a component that includes two low capacitance steering diodes with an additional low clamping TVS diode all within a 0402 package measuring only 1.0x0.6mm.

In general, capacitance and dynamic resistance are at odds with each other. The larger the diodes, the more capacitance they have, but of course the additional area can provide a low dynamic resistance. So, many times, customers have to trade off signal integrity (i.e. higher capacitance) for a lower dynamic...
Components interact with the overall system. This provided them the opportunity to gain a better understanding of the relationship between and the performance of an individual ESD component and overall system ESD immunity.

The SP3031 is now in mass production, shipping since the end of 2013. Knowing that 2015 model televisions will require a higher level of ESD immunity (possibly 6kV), Littelfuse is already working on designing a new protection component to meet this requirement by further lowering the dynamic resistance to obtain a lower clamping voltage and at the same time maintaining low capacitance and signal integrity in the system. Looking at this case study, we could conclude that preserving a smart 60-inch screen from ESD depends on 0.6mm² of silicon.

### TVS diodes provide ESD protection to fast links

Infineon Technologies’ ESD105 series of Transient Voltage Suppression (TVS) devices protect high speed interfaces of electronic systems from Electrostatic Discharge (ESD) strikes. Designed with miniaturized integrated packages for mobile devices, the ESD105 series addresses TVS for high-speed data interfaces, such as USB 3.0, Gbit Ethernet, Firewire and HDMI links used in desktop computers, TV sets and portable electronics. Being located at the surface of a device, these interfaces are especially sensitive to ESD. A mere touch of the hand can be sufficient to induce an electric current, and the energy generated by the discharge can damage the equipment or even render it completely unserviceable. With very-low clamping voltage (10V at 8kV) and ultra-low capacitance (C = 0.3pF) the ESD105 TVS diodes (single line) enable engineers to achieve strict requirements for ESD robustness and signal quality of the high-speed interfaces used in the latest generation smartphones and tablet computers. The new series provides protection that exceeds the specifications of IEC61000-4-2 in 2-pin packages (0201, 0402). The leakage current is under 20nA, contributing to longer system battery life. A dedicated pad-layout keeps PCB layout simple and minimize parasitic effects.  

**Infineon**  
[www.infineon.com/tvsdiodes](http://www.infineon.com/tvsdiodes)

### Form-in-place thermal gap filler has a thermal conductivity of 4.0 W/m-K

Gap Filler 4000 from Bergquist is the company’s latest dispensable thermal interface material, combining a thermal conductivity of 4.0 W/m-K with an extended working time of up to four hours for greater flexibility in dispensing and assembly processes. The two-part liquid material has shear thinning characteristics for optimum dispensing, and displays excellent wetting with ultra-conformability to minimise stress on components during assembly. Designed for filling unique and intricate air voids and gaps, the gap filler remains in place after dispensing and maintains its shape on the target surface. It has a low level of natural tack, and is intended for applications where a strong structural bond is not required. Cure time is 24 hours at room temperature or 30 minutes at 100°C.

**Bergquist**  
[www.bergquistcompany.com](http://www.bergquistcompany.com)

### Reinforced elastomer seals maintain surface electrical continuity at joints

Chomerics Europe’s Cho-Seal range of reinforced moulded elastomer seals are available in either conductive or non-conductive formats and are designed for use in applications such as airframes to provide EMI shielding, lightning protection, HIRF protection and radar cross-section reduction. They maintain surface continuity at joints, seams and openings in air frames. The reinforced elastomer seals consist of a corrosion resistant elastomer base with an integral woven or knitted fabric or wire mesh which gives excellent mechanical properties that allow the seals to be used in the most demanding applications. Depending on the requirements of a specific application, Chomerics can use any one of a number of its corrosion resistant silver plated aluminium and silver plated nickel filled standard Mil/Aero silicones and fluoroelastomers as the base material. Knitted Dacron fabrics dramatically increase the tensile strength of the elastomer without adding weight to the seal. For applications where high current carrying capability is required, for example to provide lightning strike protection, aluminium or wire mesh can be used. If needed other reinforcing materials can be used to give characteristics such as flame resistance.

**Chomerics**  
[www.parker.com](http://www.parker.com)
One-sided, U-shaped aluminium housing targets embedded PCs

Fischer Elektronik’s one-sided, U-shaped aluminium housing profiles have integrated, external cooling ribs for better heat conduction, interior guide ducts for slidable square nuts or threaded strips which allow attachment of the mainboard printed circuit board using length-variable spacing bolts. In addition, the lateral guide grooves integrated also into the strand profile also guarantee the acceptance of non-standardised circuit boards, electronics components or assembly plates. A 2 mm thick floor plate as well as front ceiling plates adapted to the profile contour round out this sturdy and resistant housing structure. Models with a special clamp attachment for assembly on rails for assembly in on the support rails according to DIN EN 50022 or with screwed-on attachment straps, for wall and ceiling assembly, are also offered. The embedded PC housings are available by default in three different surface models (natural colour anodised, black anodised or a combination). Additional mechanical processing, surface treatments and labelling are implemented by customer request.

Fischer Elektronik
www.fischerelektronik.de

EMI absorption sheets take out the broadband-radiated noise

Molex’ Hozox Electromagnetic Interference (EMI) absorption tape and sheets employ a unique dual-layer design to maximise the EMI noise mitigation performance. The magnetic layer’s powder composite absorbs lower frequency electromagnetic energy, while the conductive layer’s powder and high loss dielectric resin absorb high frequency electromagnetic energy. The products feature a very thin form factor and come in two different tape formats as well as an A4 sheet format, all of which can be easily die-cut to specific configurations. This dual-layer structure absorbs both the MHz and GHz electromagnetic energy effectively to provide ultra-wideband EMI noise mitigation. The tape and sheets are insulated on one side, so they can be placed in contact with any low-power active component such as noisy digital or analogue integrated circuits. While Hozox technology converts a portion of the electromagnetic waves it absorbs into heat, the amount is minimal and does not adversely affect temperature rise in the end unit, says the manufacturer.

Molex
www.molex.com

IP 30 case offers EMI protection to non-standardized PCBs

The Schroff Interscale M range of cases includes units for small and non-standardized PCBs, at a very competitive price point. The IP 30 protected cases consist of just four parts that can be easily assembled and dismantled with two screws. A total of 21 case sizes are available direct from stock. EM interference protection is provided by the interlocking case walls and offers some 20 dB at up to 2GHz. A wide range of standard accessories such as flexible board fixing, various add-on feet, a range of fans and fixing elements, allows the user to integrate their electronics quickly and simply. Removable front and rear elements give easy access to the electronics. The Schroff Interscale M case can be customized with specific case colour, cut-outs and printing on the front and rear panels. Further services include pre-fitting of all components, heat simulation using FLOWTHERM or a wind-tunnel test.

Schroff
www.schroff.co.uk
CMOS sensor supports portable HD video at 240 frames per second

With its T4K82 13-megapixel BSI CMOS image sensor, Toshiba Electronics Europe will enable smartphones and tablets to record full HD video at 240 equivalent frames per second. High-speed video recording generally results in underexposed images with short exposure times, making it difficult to increase the frame rate, explains the manufacturer. Toshiba’s T4K82 incorporates ‘Bright Mode’ technology that boosts image brightness by up to four times, realizing full HD video capture at 240 fps equivalent. ‘Bright Mode’ technology secures double the exposure time by adopting interlaced video output rather than the progressive output used by standard CMOS sensors. ‘Bright Mode’ also employs charge binning, which doubles the electrical charge of each pixel. This results in an image four times brighter than that from a CMOS sensor without ‘Bright Mode’. Toshiba will also provide an interface-progress conversion program that enables users to offer high-quality progressive video with low image deterioration, without changing the frame rate. The new sensor has a pixel pitch of 1.12μm and satisfies the 1/3.07-inch optical format.

The T4K82 incorporates ‘Bright Mode’ technology to support portable HD video recording at 240 frames per second.

Toshiba Electronics Europe
www.toshiba-components.com

Surface mount module adds IoT connectivity

The world’s first surface mount multi-chip wireless M2M module supports four different protocols to link designs easily to the Internet of Things. The ConnectCore 6 developed by Digi International provides access to all of the features of the Freescale i.MX 6 Quad, i.MX 6 Dual and i.MX 6 Solo processors for M2M applications as the small form factor and design, which requires no connectors and reduces manufacturing costs. The ConnectCore 6 modules built-in ability to connect via Wi-Fi, Bluetooth, Bluetooth Low Energy and Device Cloud by Etherios can save product designers hundreds of hours of time and expense in designing wireless devices including the pain of passing and maintaining global certifications. Complete software development tools are provided to build application software to help get products to market faster. The module has a 5-year warranty and is designed for long-term availability, ensuring that it will be available for the lifecycle of developed products. Other offerings include ConnectCore modules based on the i.MX53 and i.MX51 processor families, and the ConnectCard module-based on the i.MX28 processor. Scalable and energy-efficient, the ConnectCore family is ideal for a variety of applications. For example, the ConnectCore based on the i.MX53 processor is used to control and stream video wirelessly from the Robonaut, a humanoid robot created by NASA to assist astronauts on the International Space Station.

Digi International
www.digi.com

congatec cuts COM Express board in half

congatec has launched its first half sized COM Express module. The COM Express Mini Type 10 module, designed in the US for the German board maker, measures just 55 x 84 mm and uses Intel’s Atom E3800 ‘Bay Trail’ series of processors. The conga-MA3 comes in four different Intel Atom processor-based versions, ranging from the entry-level single-core Intel Atom E3815 with 1.46 GHz and a power consumption of 5 watts, up to the quad-core Intel Atom E3845 with 1.91 GHz and 10 watts maximum power consumption, all with an L2 cache shared by multiple cores and faster Intel HD graphics engine than the previous generation. With teh smaller board size, the lower thermal envelope is a key consideration for system architects. The Type 10 module pinout is a refresh of Type 1 and uses the single 220 pin A-B connector to take advantage of modern display interfaces. The congaMA3 can support either TMDS (HDMI/DVI) or DisplayPort as well as one LVDS channel. The conga-MA3 COM Express Mini module provides up to 8 GByte of fast DDR3L onboard memory with options for onboard eMMC as well. The eMMC supports an integrated wear levelling feature for high data security.

congatec
www.congatec.com
X-REL Semiconductor has unveiled what the company claims is the first monolithic isolated intelligent power driver for Silicon Carbide (SiC), Gallium Nitride (GaN) and Silicon power switches that is able to operate at extreme temperatures. The XTR26010 device targets motor drive, power conversion and oil and gas. Being able to properly drive normally-on (JFET, MESFET) as well as normally-off (MOSFET, JFET, BJT, SJT) transistors; the XTR26010 driver offers functional features that include isolated communication protocol between low-side and high-side drivers in order to prevent any possible cross-conduction in the application; independent monitoring of gate, drain and source terminals to detect any possible failure; on-chip Miller clamp with adjustable timing; possible pulsed drive for rapid turn-on of normally-off transistors; and on-chip soft shut-down switch. The implementation of Intelligent Power Modules (IPM) requires the minimization of parasitic inductances and capacitances between the driver and the power switch, as well as the minimization of the number of passive components to allow miniaturization as well as increased reliability. The XTR26010 is able to reliably operate from -60degC to well above +230degC, with expected lifetime of about five years at +230degC.

NFC tag powers richer user interfaces

At Embedded World, NXP was demonstrating a new kind NFC tag, the NTAG I2C, offering not only a passive NFC Forum compliant contactless interface but also an PC contact interface together with energy harvesting circuitry. Even with the appliance unplugged, the technician may figure out what the problem is and perform a firmware update, first downloaded to the user’s smartphone, then transferred to the appliance through the NFC chip to the microcontroller (powered by energy harvesting from the coil antenna as the reader is in proximity). Of course, registration and after-sales service with firmware updates could apply to just anything relying on a microcontroller, the NTAG I2C measures only 1.6x1.6x0.6mm in a quad flat package, with either 1k or 2k of user memory (of course this memory is not a limiting factor since data can be transferred directly to the appliance’s onboard memory). In fact, EnOcean’s energy harvesting switch study also demonstrated in Nuremberg was relying on this very special NFC tag for configuring the switch’s modes and functionalities during installation. This allows the installer to use the comfortable user interface of an NFC-enabled phone (the switch having none).

Intelligent power driver handles extreme temperatures

Würth Elektronik eiSos has added three new wireless power charging coils to its range of wireless power transfer coils, featuring a self-adhesive film on the back, making their assembly much easier for the user. The coils are unique with flexible ferrite shielding and are extremely thin at only 1mm. The thin and flexible carrier material is well suited for the suppression of interference above 1MHz. The charging coils have a high Q-factor and very low DC resistance, meaning that they are recommended for maximum efficiency power transfer of up to 5W.

Wireless power charging coils stick anywhere
A USB scope for Linux fans

USB oscilloscopes are popular - only that the marketable supply is focused almost exclusively to Windows platforms. Pico Technology now redeems the growing flock of Linux users by offering such a software that runs under their preferred operating system. PicoScope 6 converts a Linux PC into an oscilloscope, FFT spectrum analyser and measuring device. On-device buffering, using deep memory on some devices, ensures that the display is updated frequently and smoothly enough even on long timebases. While only the most important features from PicoScope for Windows are included — scope, spectrum and persistence modes; interactive zoom; simple, delayed and advanced triggers; automatic measurements; and signal generator control - the company assures that more functions will be added over time. Users can save captures for off-line analysis, share them with other PicoScope for Windows and PicoScope for Linux users, or export them in text, CSV and Mathworks MATLAB 4 formats. The oscilloscope software is available for Debian 7.0 (code named “wheezy”), Ubuntu 12.xx / 13.xx as well as other Debian-based distributions with mono-runtime version 2.10.81. or higher. Drivers are available for current scopes from the PicoScope 2000 to 6000 series. Again, the company said it is working to add driver support for older products. The PicoScope software requires an USB oscilloscope from the PicoScope range. Such oscilloscopes are available with bandwidths up to 1 GHz, up to 4 input channels, hardware vertical resolutions up to 16 bits, sampling rates up to 5 GS/s, buffer sizes up to 2 GS, and built-in signal generators. Other features available on some models include flexible hardware resolution, switchable bandwidth limiters, switchable high-impedance and 50 ohm inputs, and differential inputs.

Pico Technology
www.picotech.com

1.8mm thin speaker delivers 80 dB

Transducers USA's piezo ceramic MLCT (Multilayer Ceramic Transmitter) series thin speaker features a unique simple acoustic multi-layer ceramic construction that produces a high output of 80 dB from only 16V. The device’s milliwatt power consumption and high conversion efficiency in a 30x20x1.5mm package makes it suitable for flat and narrow spaces. Waterproof design and anti-electromagnetic applications make it a product of choice for digital products, household appliances, voice repeaters, or music players. The MLCT series has a wide frequency range of 300Hz to 20kHz within a working temperature range of -20 to +70°C. Units will not cause electro-magnetic interference to any surrounding electronic device as well as eliminate any such interference on its own.

Transducers USA
www.tusainc.com

Energy harvesting switch is KNX-RF ready

Cherry’s energy harvesting KNX-RF wireless switch module can directly be integrated into switches with customized control units or design-parts and requires no wires or batteries. It is designed for all switch series with a standard inner frame of 55x55mm. The actuation of the switching unit produces enough electrical energy to transmit a complete KNX-RF ready protocol in S-mode directly to any KNX-receiver. There is no need for a gateway and the configuration is done via ETS as standard. The transmitter has a range of 30m in the 868 MHz band. The radio electronics can also be used in the 915 MHz band.

Global location chip targets wearables

Adding a new level of activity and location tracking to the growing fitness and wearable device market, Broadcom Corporation claims to offer the industry’s first Global Navigation Satellite System (GNSS) system-on-chip (SoC), designed for low-power, mass-market wearable devices such as fitness trackers and smart watches. Consuming 75 percent less power than existing GNSS devices, the BCM4771 GNSS SoC with on-chip sensor hub enables consumers to more accurately track and manage their health and wellbeing by delivering precision activity tracking and location data while consuming less power than traditional architectures. This enables location intelligence and the extended battery life needed by the growing wearable market. Wearable wireless device revenues are projected to exceed $6 billion in 2018 with sports, fitness and wellness as the largest segment with 50 percent share of all device shipments, according to ABI Research. The chip constantly monitors user activity levels and location history to improve accuracy while adding advanced features such as location batching. In addition, the BCM4771 significantly reduces power consumption and board area by combining its location capabilities with an integrated sensor hub, contextual awareness, and GNSS. The SoC is complimented by the company’s Wireless Internet Connectivity for Embedded Devices (WICED™) Smart and WICED Direct software development kits (SDKs) to provide additional wireless connectivity to the platform. Designed in 40 nm process technology, the BCM4771 GNSS SoC includes a sensor hub that integrates sensor inputs for its on-chip algorithms to detect the user’s context, accurately compute speed and distance traveled, and provide fitness applications with the GNSS track. Power savings and advanced accuracy are achieved by intelligently leveraging context detection through the tight coupling of sensor inputs and GNSS on a single SoC. The device also realizes a lower overall bill of materials (BOM) cost through the integration of a multipurpose sensor hub.

Broadcom Corporation
www.broadcom.com
Wi-Fi and low power radio as plug-ins for Raspberry Pi

RS Components has added two wireless connectivity options to its portfolio of products based on the Raspberry Pi computer. The new modules are built using Wi-Fi and low power radio technology respectively and deliver wireless interface capability for mobile applications. The first module offers high-speed Wi-Fi functionality compliant with the IEEE802.11b/g/n wireless protocol via a tiny adapter that plugs into the USB port on the Raspberry Pi. The adapter supports transmission rates of up to 150Mbps. The smart adapter adjusts the transmission output according to the distance and CPU offload to achieve a reduction in power consumption of between 20% and 50%.

STM32-based Nucleo development boards compatible with Arduino

Mouser Electronics is now stocking and shipping the new Nucleo Development Boards from STMicroelectronics, for anyone to get started with ST’s STM32 product families. Besides the usual assortment of push buttons, LEDs, and a USB debug interface, Nucleo boards feature two unique sets of expansion headers. The first set of expansion headers sit on the outside edges of the board, and are standard headers on all Nucleo boards. The second set of expansion headers are nestled inside the first set and are Arduino shield compatible.

Multi-touch PCT technology takes up to 40 contact points

MSC Technologies now stocks Zytronic’s Multi-touch Projected Capacitive Technology (MPCT), supporting up to 40 independent contact points to be analysed simultaneously on displays of up to 85". This multi-touch technology is based on Zytronic’s ZXY200 and forthcoming ZXY300 touch controllers and a robust scalable touch sensor. It uses a matrix of copper electrodes of 10 µm in diameter which are located in impact and scratch-proof glass laminate of several millimeter thickness. A palm rejection function differentiates between deliberate and erroneous contact with the touch panel. The sensor even works when wet, dirty or touched with gloves. Users can also access the controller firmware and adjust the sensitivity themselves. This allows the sensor to be precisely adjusted to the respective requirements of the system design.

4.8” TFT display packs 720x1280 pixels with wide viewing angles

Japanese manufacturer of TFT modules Ortustech Technology is offering a wide product range of small and medium sized TFTs from 5.1 cm (2.0”) up to 17.78 cm (7.0”) screen sizes distributed by Data Modul. The 4.8” TFT COM43H4M87ULC unit in particular boasts a very high resolution of 720x1280 dots, supporting a very sharp and crystal clear image. The pixel structure is not visible for the human eye, whilst the viewing angles of L/R/U/D 80°/80°/80°/80° make the TFT readable from all directions. The blanview technology also makes the TFT readable under sunlight conditions. The unit measures 63.7x115.6mm for a thickness of only 1.6 mm.

M2M module offers cost-effective migration from 2G to 3G

From distributor MSC, the Quectel UC15 3G-Module provides cost-effective migration from 2G to 3G. The module is UMTS/HSDPA-capable and is pin-compatible to the same company’s M10- and M12-GPRS Class 12-Modules. Covering bands from 900 to 2100 MHz for multiband-W-CDMA and 850/1900-MHz quad-band-GSM, the module, measuring 29 x 29 mm, is downwards compatible to EDGE and GPRS with Multi-Slot Class 12. UC15 has power consumption of 3.5 mA in sleep mode, and 520 mA maximum in UMTS mode. Interfaces include USB, UART, PCM as well as two analogue I/Os and ADC-channels. The maximum download speed is 3.6 MBit/sec and the transfer rate at upload is 384 kbit/sec.

Instant global positioning from a 22x22x8mm GPS antenna module

New to the Alpha Micro product portfolio is the u-blox PAM-7Q GPS/QZSS antenna module measuring 22x22x8mm. The device integrates a satellite receiver IC plus all passives and a pre-tuned GPS antenna in one single compact package. Designed for applications such as portable, covert tracking, asset-tracking, animal and child tracking devices, this new module combines low-power consumption with high-sensitivity, sophisticated noise suppression and I2C / UART interfaces, making the integration of global positioning as simple as possible. PAM-7Q can easily be integrated into pre-existing designs or soldered with a pin-header to a customized PCB. The 18x18mm patch antenna is designed for optimal antenna performance independent of orientation.

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4.8” TFT display packs 720x1280 pixels with wide viewing angles

Japanese manufacturer of TFT modules Ortustech Technology is offering a wide product range of small and medium sized TFTs from 5.1 cm (2.0”) up to 17.78 cm (7.0”) screen sizes distributed by Data Modul. The 4.8” TFT COM43H4M87ULC unit in particular boasts a very high resolution of 720x1280 dots, supporting a very sharp and crystal clear image. The pixel structure is not visible for the human eye, whilst the viewing angles of L/R/U/D 80°/80°/80°/80° make the TFT readable from all directions. The blanview technology also makes the TFT readable under sunlight conditions. The unit measures 63.7x115.6mm for a thickness of only 1.6 mm.

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By Christoph Hammerschmidt

APPLE, TESLA, THE PERFECT COUPLE?

IN THE LAST few days, reports on a potential liaison between Apple and electric carmaker Tesla elicited a strong echo in the media. These reports are just the distant harbingers of a major shake-up in the automotive industry.

The San Francisco Chronicle got the ball rolling when it published a report about a meeting between Tesla CEO Elon Musk and Apple’s Adrian Perica who oversees the computer giant’s acquisitions.

Though the meeting took place already in April 2013, the Silicon Valley seismometers are extremely sensitive (a late result of Andy Grove’s statement that “Only the Paranoid Survive”) and the report created quite a stir.

Now Tesla’s Musk - probably against his intention - poured oil into the flames when he declined a blunt denial in a Bloomberg TV interview upon the question if Tesla is for sale. Instead, he manoeuvred around - he admitted that there have been talks between Tesla and Apple but he declined to elaborate.

When the interviewer put him the direct question “Are you for sale”, he did not answer with a clear “yes” or “no” but instead he said that “such a sale would be very unlikely”, leaving lots of space for the interested public to speculate over his real intentions.

But a sale of Tesla to Apple is not so much the question. The simple fact that an IT company and a carmaker are discussing anything that might be even distantly related to an acquisition is per se very remarkable. Things are becoming a bit more plausible if one takes into consideration that Apple is not just a manufacturer of conventional cars.

It has to be an electric car company (for the reasons described above) and it has to be self-assertive as Apple. The latter condition, by the way, rules out more or less all established carmakers - in particular the German premium players who never would bow to an IT company.

“Apple is the icon of the digital lifestyle, and in one sense Tesla is not much different - electric cars are an emerging symbol for a new kind of mobility.”

Analysts label cars (and even more so, electric cars) as “the ultimate mobile terminal” for IT services, it is just logical that IT technology players increasingly watch out for opportunities to occupy this promising market place.

Cars, and again: even more so, electric cars, will be the place to offer IT-based services of the future. This starts with navigation-related services (location-based online advertising, for instance), continues with behaviour-based, pay-as-you-drive car insurance and enhanced real-time traffic information and does not end with multi-modal transport.

Of course, all these services require hardware, software and wireless communications. But these elements are just the technological foundations for new business models. It is no wonder that it was just business model innovator Google who came up as the first IT company with the idea of selling (automatic) cars, and I am sure we will witness more moves from this side.

But, back to our original question: Would Tesla and Apple be the perfect couple? There have been repeated rumours that BMW aired a similar interest already years ago - something the carmaker does not comment either, much like Tesla’s founder Elon Musk in his recent Bloomberg interview. To me, one thing is clear: The perfect partner for Apple will not just be a manufacturer of conventional cars. It has to be an electric car company (for the reasons described above) and it has to be a company with strong intellectual and emotional ties into IT and digital thinking.

Plus, it has to be someone who does not insist in calling the tune in the duo with a company as self-assertive as Apple. The latter condition, by the way, rules out more or less all established carmakers - in particular the German premium players who never would bow to an IT company.

Well, that is: for the time being. The IT race in the automotive realm is on. No matter how the outcome in the affair between Tesla and Apple: We will see more of them. And this could easily change the balance of power between IT-related service providers and traditional carmakers, premium or not.
Putting FPGAs to Work in Software Radio Systems Handbook

FPGAs have become an increasingly important resource for software radio systems. Programmable logic technology now offers significant advantages for implementing software radio functions such as DDCs (Digital Downconverters). For many applications, this implementation shift brings advantages that include higher precision processing, higher channel density, lower power, and lower cost. Recently updated to its 7th edition, this handbook introduces the basics of FPGA technology and its relationship to SDR systems.


Real-Time Spectrum Analysis for Troubleshooting 802.11n/ac WLAN Devices

802.11 WLAN devices operate in the license-exempt 2.4 GHz ISM and 5 GHz UNII bands, where they must share spectrum with many other wireless devices that can cause interference. Verifying the performance of WLAN devices in the presence of interfering signals that may be time-varying is an important part of design verification. Troubleshooting performance problems in real-world environments is another challenge, and being able to capture interfering signals that may be present and impacting performance, even if they are transient and very short in duration, can provide important insight. Real-time spectrum analysis can help address these test challenges.


NSR Noise Suppressors: Wirewound Resistors

Noise suppressors are wire-wound resistors which are specially designed to be implemented in automotive ignition systems to reduce radio frequency interference (RFI) caused by electrical discharges. The resistors can be placed in the rotor of the distributor, the spark plug leads, as well as in the spark plug caps itself. This application note will explore key specifications of the devices.


Radar Waveforms for A&D and Automotive Radar

This white paper provides a detailed view on radar waveforms for Aerospace and Defense and commercial radar systems. Waveforms such as pulse and pulse-Doppler signal, continuous wave and frequency shift keying waveforms are described. It also shows continuous waveform trends designed for specific needs and application differences of continuous wave radar compared to pulse radar systems.


Hall-Effect Sensor ICs for Motor Control

Motor control circuits in appliances, including refrigerators, washing machines, and air conditioners, need to operate more efficiently, reliably, and safely, while meeting cost requirements. With energy efficiency becoming a greater concern, appliance manufacturers should consider Hall-effect current sensor ICs for motor control.


Understanding WLAN offload in cellular networks

The coming challenge for Wi-Fi™ offload is to provide a converged network solution for a seamless, transparent and better user experience. The user will not have to interact with its smartphone or mobile device in any way to switch from 3G/LTE to Wi-Fi™. The data stream will even be able to use both connections at the same time depending on QoS requirements. This short guide explores the technical aspects of Wi-Fi™ offload architecture and its related capabilities. It is presenting the different types of possible integration into existing mobile networks to provide a viable and efficient way to offload subscriber traffic. It concludes with an overview on testing methods.
650V TRENCHSTOP™ 5
A Technology to Match Tomorrow’s High Efficiency Demands

The TRENCHSTOP™ 5 IGBT technology from Infineon redefines the “Best-in-Class IGBT” by providing unmatched performance in terms of efficiency. When high efficiency, lower system costs and increased reliability are demanded, TRENCHSTOP™ 5 is the only option. The devices deliver a dramatic reduction in switching and conduction losses whilst also offering a 650V blocking voltage.

Key features and benefits
- New benchmark in terms of Best-in-Class efficiency
- Lowest ever switching losses
- $V_{CE(sat)}$ more than 10% lower than previous generation
- Temperature stable $V_f$ value of free-wheeling Rapid diode
- 2.5 factor lower $Q_g$ compared to HighSpeed 3

www.infineon.com/trenchstop5