Inlays add focussed PCB performance
High density PCB enabled by “X-in-Board” technology

Advanced PCBs fabricated by AT&S (Leoben, Austria) can employ the company’s X-in-Board technology that involves embedding of special technologies (inlays) in standard PCBs. AT&S has observed that while it can offer a range of special processes, materials and technologies that are optimized for specific requirements such as high-density wiring, enhanced thermal performance or high frequency (HF), many real-world designs only need these high-performance, but more expensive, technologies in small areas of the PCB. The technology combines low-cost standard boards with the relevant higher-priced, high-end technologies – but only where they are needed. Elements with high-density wiring (multi-layer inlays) can be partially integrated directly into the overall structure, so the designer can reduce the overall PCB thickness. For HF applications such as radar systems in automobiles, special HF inlays can be integrated (for example, based on ceramic materials). X-in-Board technology can assist with heat management, for example in the case of high-power LEDs in the automotive sector that place greater thermal demands on the PCBs. Using metal core PCBs based on IMS (insulated metal substrate) or solid copper (Cu) components as an inlay (as pictured) allows optimal thermal transfer through the PCB, and means that power electronics and control electronics can be combined. Full item here.

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Late in November, the State of South Australia put into service “the world’s largest battery”, built by Tesla. The installation is a 100 MW (power delivery rate) and 129 MWh (capacity) array of lithium ion cells, with attendant inverters, that has been designed to support the local electricity grid.

Australia has one of the world’s most urbanised populations; most of its citizens live in just a handful of cities, that are very widely separated. Electricity supply infrastructure, historically, evolved on a state-by-state basis and interconnections that might provide a resilient national grid are limited. Peak loading occurs in the summer months, with maximum air conditioning use, and temperatures that are potentially hazardous to the health of vulnerable sections of the community in the absence of air conditioning occur regularly.

In 2016, the State suffered a series of major power outages, storm damage coinciding with the season of peak loading, and sought a means of regulating the peaks load on its grid. As part of the specification, South Australia’s authorities wanted the facility up-and-running before midsummer, 2017/18. Tesla won that contract with CEO Elon Musk making a, “fast or free” promise – that Tesla would build and commission the facility in 100 days, or it would be free. That target was achieved with the switch-on in November, of the array of 396 interlinked battery units.

The installation has been placed adjacent to a windfarm close to the town of Jamestown, around 220 km inland of state capital Adelaide. South Australia has made a major investment in renewable energy, with over 40% of the its electricity coming from that source – predominantly, from wind turbines. However, the topic is controversial. A large and vocal constituency – that appears to include a climate-change-sceptic element – argues that the investment in wind has been overdone relative to conventional sources. Despite being a major supplier of uranium, Australia has no nuclear power generation and other than wind and solar, its electricity is entirely from fossil-fuel sources.

The energy reserve built by Tesla has been widely described in “energy storage” terms. However, even though 129 MWh is impressive, that will not go far in supporting the load presented by a large city when the wind falls light. For the moment, the main contribution of the facility is likely to be in managing short-term peak loads, and in ensuring grid stability.

The price paid for the installation has not been disclosed; nor is it clear if Musk’s lithium-ion-battery Gigafactory has yet scaled up to the point where a single order of 129 MWh in three months can be handled as run-of-production. Some reports refer to an output capacity target for 2018 of 35 GWh/year. From this, if achieved, Tesla has to supply its existing and new vehicle production, including its recently-announced “semi” (articulated truck); and the business Musk is trying to build in domestic and commercial energy storage with its Powerpack and Powerwall products.

Once again, and as noted before in this column, this is classic Musk/Tesla. Faced with the variability of supply from renewable resources, a “traditional” (for the lack of a better term) viewpoint might be to say that we do not have the battery technology we need to build useable and useful energy stores, on a grid-power scale. This project says, in contrast, that what we have available today is more than good enough to do something useful – so let’s go with what we have, and develop it as far as it’s capable of being taken.

Serried ranks of white cabinets in a paddock in South Australia may, or may not, be a pointer to part of our energy supply security in the future: but its performance is sure to be closely scrutinised by operators around the world, as we edge towards a more intermittent, and more distributed, energy supply base.
world of wired & wireless components

SimpleLink™
MSP432
Ethernet MCU

25 functions for 25 cents
MSP430™
Value Line Sensing MCUs
Pico Technology (St. Neots, UK) has added three 15 GHz models and a further 25 GHz model to its portable and low-cost PicoScope 9300 series of USB sampling oscilloscopes. The 15 GHz models replace the preceding 9200 Series 12 GHz models, with significantly upgraded specifications at lower prices.

All Pico Sampling Oscilloscopes now operate under the PicoSample 3 software. These instruments combine Pico’s sampling technology with interface via USB and LAN control ports. At an entry-level price below $11,000, the 9301-15 has two channels at 15 GHz bandwidth and prescaled trigger to 14 GHz. It delivers 16-bit sampling rate of 1 Msample/sec in support of fast-update eye diagrams, persisted traces, histogramming and statistical analysis. Equivalent sampling rate tops out at 15 Tsample/sec — a time resolution of 64 fsec — along with a long maximum trace length for sampling oscilloscopes of up to 32 kilosamples.

At 15 GHz the entry-level sampling oscilloscope aligns with today’s popular gigabit data rates. 15 GHz bandwidth will support third harmonic characterization of serial data out to 10 Gb/sec and fifth harmonic out to 6 Gb/sec. Full touch screen control, menus that configure to the application at hand, comprehensive PRBS pattern lock, and eye-line step and scan, support visualization, measurement and characterization of high-speed serial data.

The third of the new 15 GHz models, priced below $15k, the 9311-15 addresses single-ended Time Domain Transmission and Time Domain Reflection measurements, with an upgrade to the predecessor 9211 in cable, component, backplane and PCB impedance and transmission characterizations and network analysis. In this model, system transition time (65 psec) halves distance resolution and adjustable pulse width extends reflected fault detection range from around 4 mm typically out to 400m. At 20 GHz, the 9311-20 continues to support fully differential and deskewable TDR/TDT capability and all 9300 models can be paired with the PG900 standalone fast pulse generators to achieve similar TDR/TDT capability, for example on the four-channel and optical input models, or greater flexibility with any 9300 model.

At 25 GHz, Pico has created the model 9302-25 to add 11.3 Gb/sec clock recovery to the higher bandwidth models. This bandwidth will support 5th harmonic assessments at data rates to 10 Gb/sec and, assuming a clock or sub-clock is available, 16 Gb/sec at 3rd harmonic.
TI adds wired-Ethernet connectivity to SimpleLink MCU range

TI’s latest addition to its SimpleLink microcontroller series is a version that has on-chip MAC and PHY to directly connect to a wired 10/100 Ethernet link, enabling designers to, “merge the worlds of wired and wireless connectivity by connecting sensors to the cloud.”

The added parts will, TI says, simplify industrial gateway designs, making use of full code compatibility across the SimpleLink MCU platform, which is now a single hardware, software and tool platform for wired and wireless MCUs. MSP432 Ethernet MCUs are based on a 120-MHz Arm Cortex-M4F core with an integrated MAC and PHY, together with USB, Controller Area Network (CAN) and advanced cryptography accelerators, with the designation MSP432E411Y. Designers can combine wired communications with the SimpleLink MSP432 host MCUs through integrated serial interfaces with wireless connectivity technology such as Sub-1 GHz, Wi-Fi and Bluetooth to connect end nodes to the cloud using the SimpleLink software development kit (SDK). The same code base can be employed when designing end nodes and intelligent gateways.

Wireless sensor networks built on SimpleLink wireless MCUs can connect up to 50 secure sensor nodes to a gateway. The gateway, based on the SimpleLink Ethernet MSP432E4 MCUs, acts as a centralized management console to process and aggregate data and deliver it to the cloud via Ethernet for additional data analysis, visualization and storage. The chip comes with its own development starter kit; the MSP432E401Y MCU LaunchPad development kit is priced at $19.99. The device itself is $9.00 (1000).
Intel Management Engine flaws affect latest processors  by William Wong

The Intel Management Engine is software found in its latest processors, and it has problems—a lot of them. How many operating systems are running on your Intel machines? Probably more than you might think. There’s the BIOS/UEFI system used to boot most systems, for starters, which is essentially an operating system. Underneath the hood of most new Intel processors is another operating system called the Intel Management Engine (ME). It has at least 11 major security flaws in it according to this report. At this point, the ME issue affects the 6th, 7th, and 8th Generation Intel Core family; the Xeon Processor E3-1200 v5 and v6 family; the Xeon Processor Scalable family; the Xeon Processor W family; the Atom C3000 Processor family; the Apollo Lake Intel Atom Processor E3900 series; the Apollo Lake Intel Pentium series; and the Celeron N and J series.

Intel has provided a detection tool for Windows and Linux that will indicate whether a chip has the identified issues. Fixes have been released by Intel through a number of vendors whose BIOS/UEFI updates address the problem. There is also an undocumented process for disabling ME.

24 GHz radar, movement & speed detection evaluation kit

Distributor Aspen Electronics (Ruislip, UK) has the K-LD2 Evaluation Kit from RFbeam Microwave (St. Gallen, Switzerland), supplier of planar radar sensors, K-band measuring equipment and engineering. Typical applications for the K-LD2 include movement detection and speed measurement. The K-LD2 Evaluation Kit is a fully operational 24 GHz radar movement detector allowing development engineers to quickly evaluate this technology. The K-LD2 24GHz radar module plus a Digital Signal Processing chip provides users with a more complete solution than the radar module alone. This will allow those interested in “radar motion sensing” to make better use of the technology as this offering represents a much simpler solution when compared to the prospect of using a radar module and developing your own signal processing algorithms. The K-LD2 sensor supplied with the kit is a fully digital and low-cost radar movement detector. The sensor features a 2 x 4 patch antenna radar front-end with an asymmetrical beam and a signal processing unit with two digital outputs for signal detection information. The evaluation board visualises the two digital outputs of the K-LD2 using two LEDs. The sensitivity and the hold time are adjustable using analogue inputs with potentiometers. A serial interface features a powerful command set to read-out advanced detection data or to fully customise the detection algorithm. The digital structure simplifies use in any stand-alone or MCU based application where a movement detection or speed measurement is required.
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Melexis’ MLX90632 SMD device is, the company says, a ‘disruptive’ and thermally robust solution for multiple applications; it measures in the far-infrared (FIR) part of the spectrum and can be used in a wide range of applications where accurate non-contact temperature measurement is required.

The MLX90632 family is based on Melexis' FIR technology; employing an ultra-small integrated thermopile, the CMOS IC is a complete solution in a single 3 x 3 x 1 mm QFN package including the sensor element, signal processing, digital interface and optics, for rapid and simple integration. Ambient light is screened out by an optical filter that passes 2 – 14 µm wavelengths. The chip operates from 3.3V (typical) and delivers measured data over I2C to an external microcontroller. It uses 1 mA active, and under 2.5 µA in standby. The device is factory calibrated with calibration constants stored in an EEPROM memory. Ambient and object temperature can be calculated based on these calibration constants and the measurement data. Factory calibrated in the ambient temperature range is from -20 to 85˚C and in the object range, from -20 to 200˚C. It is capable of measurement resolution of 0.02C, and accuracy is ±1˚C within the object temperature range of 0 to 50˚C, for consumer applications.

The accurate device delivers high levels of thermal stability when experiencing thermal gradients and rapid temperature changes, solving a well-known weakness of existing infrared sensors. It occupies a surface mounted (SMD) package compatible with standard PCB assembly techniques. First released in a commercial grade version, future versions of the MLX90632 will address, amongst others, medical applications.

Maxim renews secure-authentication IC line with its own PUF technology

Maxim Integrated has disclosed details of its latest secure authentication chip, for which the company has developed its own technology for physically unclonable functions (PUFs) as the most secure method of storing encryption keys within a device. Maxim has a well-established product line of security-oriented devices, including the secure authentication devices it acquired with the purchase of Dallas Semiconductor. Its latest introduction in that family is the DS28E38 secure authenticator with technology Maxim is branding as “ChipDNA”. This will, Maxim asserts, assist designers to inexpensively protect their intellectual property and products with a solution immune to invasive physical attacks.

New in this generation of device is Maxim’s version of the PUF function. A PUF exploits process variations inherent in the semiconductor manufacturing process that render each individual IC unique. In perhaps the best-known such technology to date, the IP developed and licensed by IntrinsicID, an SRAM array is the medium, and the state in which it “wakes” on power-up provides the unique signature. Maxim has taken an alternative approach, and uses fundamental parameters, threshold voltages, of individual transistors – and tolerance therein – to generate the unique fingerprint of
each device. That in turn is used to generate a cryptographic key – the critical point being that the key only exists for as long as an authentication-request cycle is in progress; is not stored anywhere; and is not available to be accessed or hacked. Having created a key, the secure authenticator takes its place in a conventional public/private key scheme – but provides that scheme with uniqueness, and repeatability. It may be, for example, be used to sign hashed data to verify the authenticity of a transmission.

If the DS28E38 were to come under an invasive physical attack, the attack would cause the sensitive electrical characteristics of the circuit to change, further impeding the breach. In addition to the protection benefits, ChipDNA technology simplifies or eliminates the need for complicated secure IC key management as the key can be used directly for cryptographic operations. The ChipDNA circuit has also demonstrated high reliability over process, voltage, temperature, and aging. Additionally, to address cryptographic quality, PUF output evaluation to the NIST-based randomness test suite was successful with pass results.

Using the DS28E38, engineers can, from the start, build into their designs a defence against hacking. The IC is low-cost and simple to integrate into a customer’s design via Maxim’s single-contact 1-Wire interface combined with a low-complexity fixed-function command set including cryptographic operations. The DS28E38, in a 3 x 3 mm 6-pin TDFN package, costs $0.83 (1000). An evaluation kit is available for $65.00.

Noise-tolerant op-amps for automotive sensing - “a first”, says Rohm

With its BA8290xYxx-C series, Rohm Semiconductor is offering automotive-grade op-amps with “unprecedented” noise immunity, that contributes to improved reliability and simpler designs in automotive sensor applications and allows the designer to reduce the amount of additional filtering required. Output voltage fluctuations are suppressed in all frequency bands to less than ±1%, compared to ±3.5% to ±10% with conventional amplifiers. This allows, for example, sensor signals to be amplified without the need for noise countermeasures, which significantly reduces design load and contributes to greater reliability. The new series is suited for automotive applications, where sensors are used along with the core systems for electric vehicles (EV) and hybrid electric vehicles (HEV).

The BA8290xYxx-C series combines circuit design expertise (new noise countermeasures circuit), layout (based on mar-
ket-proven analogue expertise) and use of bipolar processes. This approach reduces the number of components required for noise suppression (three RC filters for input, output and power supply), and also meets noise-related challenges in the development of automotive electrical systems, whilst contributing to lighter design load and higher reliability. Rohm is also developing high noise immunity op-amps for the industrial market. The BA8290xYxx-C series is AEC-Q100 qualified for automotive applications. It is characterised by a low current consumption of 0.5 mA (BA82904YF-C/BA82904YFVM-C) and/or 0.7 mA (BA82902YF-C/BA82902YFVM-C). The ICs are available in four versions with two or four op-amps and a supply voltage range from 3.0V to 36V. Their input offset voltage is typically around ±2 mV and/or a maximum of ±6 mV, the input voltage range between VEE and VCC-1.5V. The operating temperature range is –40°C to +125°C. Package versions, SOP8 (BA82904YF), MSOP8 (BA82904YFVM-C), SOP14 (BA82902YF-C) and SSOP-B14 (BA82902YFVM-C) are available. The pin-compatible packages can directly replace existing standard products.

Laser-based “no-touch” touch sensor system

Distributor Digi-Key has Neonode Inc.’s zForce AIR Touch Sensors, that claim a number of advantages over traditional touch technologies such as resistive, capacitive and camera-based solutions. zForce AIR Touch Sensors enable touch interaction on any type of display or surface of any shape, to add interactivity and differentiation to products with or without displays. zForce AIR Touch Sensor is a laser light based touch sensor that can be integrated and used in various applications. The sensor characteristics are high scanning frequency, low latency and good touch accuracy without the need for calibration. Touch functionality is provided without any glass or plastic film overlay. The result is a 100% optical transparency with consistent display image quality and no disturbing glare.

AIR Touch Sensors are intended for integration in a wide range of applications, such as: PCs/Tablets, TVs/monitors, printers, mechanical key replacement, white goods, smart furniture, interactive mirrors, ATM/POS terminals and many forms of control panel.
“Most advanced” C/C++ compiler for embedded/IoT processors - GHS

From Green Hills Software, the latest release of its C/C++ compilers combines certified safety with what the company claims as the highest 64-bit performance and programmer productivity for critical software. These latest optimising C and C++ compilers, version 2017.5, are available for 32-bit and 64-bit embedded processor architectures, including Arm, Intel and Power Architecture. Highlights include C/C++ functional safety certification, up to 30% higher performance, and more compatibility with third-party tools.

Green Hills Optimising Compilers have implemented both general-purpose compiler optimisations and CPU-specific optimisations to enable C and C++ developers to extract the most from purpose-built features of 37 processor architectures. Compiler 2017.5 supports the leading embedded architectures including Arm, Intel, Power Architecture, Renesas RH850, MIPS, ColdFire and Tri-Core, delivering the highest performance to date:
- Maximum performance 16-50% higher as measured over industry and customer benchmarks, improving on results from GNU and LLVM compilers
- New support keeping pace with the latest architecture extensions for Armv8-A, Armv8-R and Armv8-M, including new security instructions
- Improved control and utilisation of CPU pipeline architectures, floating point optimisations and opcode utilisation
- Enhanced control for auto-vectorization of leading SIMD instruction extensions including Arm NEON and Intel Streaming SIMD Extensions (SSE)

Green Hills C/C++ Optimising Compilers 2017.5 are certified as qualified tools at the highest levels of functional safety for automotive (ISO 26262 ASIL D), industrial (IEC 61508 SIL 3) and railway (EN 50128 SWSIL 4). In addition, the integrated single-pass MISRA-C adherence checker gives development teams a flexible means to prevent new bugs and enforce cleaner, higher-quality code. Green Hills compilers are also tightly integrated into the Double-Check static analysis tool that performs full program analysis in a single pass, finding bugs caused by complex interactions between pieces of code across many source files.

STM32 MCU range extension focusses on low-power “smart objects”

Next-generation ‘smart objects’ can do more and consume less with STMicroelectronics’ STM32L4+ MCUs. Large memory and new graphics – including specific support for ‘smart-watch’-style displays – meet the needs of wearables. With features such as an advanced controller, optimized for small, circular displays, that boosts pixel-handling efficiency; and a power-saving architecture enabling richer functionality with longer battery life, this new generation of the STM32L4 series stretches performance to 150 DMIPS (233 ULPMark-CP) at 120 MHz. The MCUs can be the central controller in a full range of fitness bands, smart watches, small medical equipment, smart meters, and smart industrial sensors. All these applications require sophisticated functions, instant responses, and minimal downtime for battery charging, matched by the ultra-efficient STM32L4+. STM32L4+ has processor performance together with the largest on-chip memory for this type of ultra-low-power microcontroller,
and the most advanced graphics capabilities for smooth and fluid user experiences. The new Chrom-GRC graphics controller can handle circular displays (TFT-LCDs) just as efficiently as square ones, without wasting resources managing pixels that are never displayed. Also on-chip is ST’s innovative Chrom-ART Accelerator, which enhances graphics performance. The enhanced memory capabilities include dual Octo SPI ports, making these the first STM32 devices to support this interface. The dual ports allow cost-effective and high-speed extension of code or data storage using single/dual/quad/octal SPI, or HyperBus, Flash or SRAM memories. The advanced power-saving technologies include proprietary FlexPower-Control, which protects important data like SRAM contents and I/O-pin states when the device is in low-power modes. FlexPower-Control also provides for separate power-supply domains that allow individual voltage adjustment and power-down to meet processing loads at the lowest possible energy, and a programmable high-accuracy clock that saves external components and minimizes power consumption.

Researcher builds supercomputer with Raspberry Pi boards   by Nick Flaherty

A researcher at the Los Alamos National Laboratory in the US has developed an affordable, scalable supercomputer system using thousands of inexpensive Raspberry Pi nodes, that will be used to evaluate strategies for loading very large compute problems on to very-many-core machines. The system brings a powerful high-performance-computing testbed to system-software developers and researchers while reducing the cost and power consumption compared to other HPC systems by using boards from the Raspberry Pi Foundation in Cambridge. "It’s not like you can keep a petascale machine around for R&D work in scalable systems software," said Gary Grider, leader of the High Performance Computing Division at Los Alamos National Laboratory, which hosts the Trinity supercomputer. "The Raspberry Pi modules let developers figure out how to write this software and get it to work reliably without having a dedicated testbed of the same size, which would cost a quarter billion dollars and use 25 megawatts of electricity." Australian company BitScope Designs (www.bitscope.com.au), developer of BitScope Blade, an infrastructure platform for Raspberry Pi available globally via [distributor] element14, built a large Raspberry Pi cluster for the pilot conceived at Los Alamos National Laboratory (LANL), and with collaboration by SICORP of Albuquerque, New Mexico. The system consists of five rack-mounted Pi Cluster Modules, each with 150 four-core nodes of Raspberry Pi ARM
processor boards. They are fully integrated with network switching infrastructure. With a total of 750 CPUs with 3,000 cores, the system gives developers exclusive time on an inexpensive but highly parallelized platform for test and validation of scalable systems software technologies. The whole system uses 2.2kW.

8-bit PICs use independent peripherals to speed CAN bus response

Microchip’s PIC18 K83 microcontroller family, the company asserts, makes CAN-based designs simpler and more cost effective: the 8-bit device incorporates Core Independent Peripherals to provide deterministic response to real-time events for faster response time. Implemented in hardware, Core Independent Peripherals can reduce design time with fast configuration, removing the need to write and verify additional software. Functions can be configured through the MPLAB Code Configurator (MCC) tool. The family is suitable for applications using CAN in the medical, industrial and automotive markets. The PIC18 K83 devices contain 15 time-saving CIPs including: Cyclic Redundancy Check (CRC) with memory scan for ensuring the integrity of non-volatile memory; Direct Memory Access (DMA) enabling data transfers between memory and peripherals without CPU involvement; Windowed Watchdog Timer (WWDT) for triggering system resets; 12-bit Analogue-to-Digital Converter with Computation (ADC2) for automating analogue signal analysis for real-time system response; and Complementary Waveform Generator (CWG) enabling high-efficiency synchronous switching for motor control. The PIC18F25K83 with 32 kB of Flash memory, and PIC18F26K83 with 64 kB of Flash memory, are each available in 28-pin SPDIP, SOIC, SSOP, UQFN and QFN packages.

Autonomous machines navigate with industrial inertial measurement units

Analog Devices (ADI) has added five high-performance inertial measurement units (IMUs) that address the navigation- and safety-related needs of industrial applications in a range of emerging markets, while also reducing their system complexity and cost. The ADIS16470, ADIS16475 and ADIS16477 IMUs are small, surface mount devices spanning a range of performance, cost, and application-suitability needs. The ADIS16465 and ADIS16467 IMUs offer similar performance advantages in a more ruggedized enclosure option. They offer a new level of performance-for-cost ratio to unmanned aerial vehicle (UAV) applications where consumer grade sensors have fallen short of ideal performance and have failed to meet reliability goals. These new IMUs bring the same benefits to
Autonomous Machine applications in fields such as Smart Agriculture where the demands of such rugged equipment previously forced a choice between cost-challenged, highest-grade sensors or performance-limited commercial sensors. All of the IMUs provide six degree-of-freedom (DoF) sensing via triple-axis MEMS-based accelerometers and gyroscopes, and are focused on the demands of the Industrial "Internet of Moving Things" and its need for precise geolocation. Their performance allows systems to characterize motion accurately despite turbulence, vibration, wind, temperature, and other environmental disturbances, resulting in more-accurate navigation and guidance, and/or instrument stabilization. These high-grade sensors reduce or eliminate the need to improve performance via added test, components, calibration, or software measures. The ADIS1646x and ADIS1647x IMUs are specifically designed to reject what are otherwise significant error sources, such as ‘g’-influence, cross-axis sensitivity, and temperature and mechanical stress related drifts.

Texas Instruments has introduced its “lowest-cost ultra-low-power MSP430 microcontrollers” for sensing applications, under the slogan “25 functions for 25 cents”. The MCUs feature FRAM (ferroelectric, non-volatile, RAM). The focus on sensing applications comes with the presence on the respective MCU chips of analogue/mixed-signal functions: the price point (in US cents) is for volume buys of the smallest device in the family ($0.29 and up in more modest volumes). The 25 functions part of the tag line refers to the support that TI is adding in the shape of a library of basic software functions – timers, I/O routines, and the like, that you can patch into application code, or modify according to specific needs. The introduction will be supported by a new, entry-level LaunchPad development board – this will be available until year-end (2017) at a price that echoes the family designation ($4.30 and at $9.99 thereafter. At launch, there are two specific, entry-level family members in this MSP430 “Value Line”: the MSP430FR2000 and MSP430FR2100, with 0.5 kB and 1 kB of FRAM, respectively; the second of these has an on-chip 1-bit A/D converter. Packaging is in 3 x 3 mm VQFN; or – offering simple development for those without fine-line surface mount tooling – in TSSOP. The -2000 and -2100 parts have, TI acknowledges, “few peripherals” – however, they maintain compatibility with more complex MCUs in the family. The software support takes the form of a collection of 25, 2-page app notes, each on a basic function such as timers, input/output expanders, system reset control-
Intels latest mobile Core processor includes AMD graphics

In a partnership that would at one time have seemed improbable, Intel has announced that it will introduce a compute module in its 8th generation Core line-up, that will incorporate an AMD Radeon graphics processing chip. With some echoes of the days of Pentium II, which came in a slot-based multi-chip module – but greatly updated to current technology – the mobile-computing oriented multi-chip module uses a technology Intel is calling EMIB. Embedded multi-die interconnect bridge appears to be a high-speed data path, or perhaps an interposer (but not, says the Intel video clip, a ‘standard interposer’), integrated in the multi-chip substrate to tightly couple the processor core and the graphics chip. Also on the same high-speed interconnect is a vertical stack of graphics memory chips. The combination is pitched as providing a high-performance but thinner package to offer more advanced graphics in smaller, lighter portable platforms, with Intel Core H-series processor, second generation High Bandwidth Memory (HBM2) and a custom-to-Intel, third-party discrete graphics chip from AMD’s Radeon Technologies Group – all in a single processor package. An AMD spokesman describes the graphics chip as a “semi-custom” implementation, developed with and specific to, the Intel module. The design and packaging innovations, Intel asserts, reduce silicon footprint by more than 50%, and enable real time power sharing across CPU and GPU for best performance.
The latest update of the Arduino Create web platform enables development and deployment of IoT applications with integrated cloud services on Linux devices. The initial supported devices are based on the Intel x86* architectures although the plan is to expand support to all major hardware architectures. Arduino has announced the release of a set of new features for its Create Cloud platform (create.arduino.cc) aimed at expanding the number of Arduino supported platforms for the development of IoT applications. Arduino Create Cloud users can now program Linux boards as if they were regular Arduino boards. Multiple Arduino programs can run simultaneously on a Linux based board and programs can communicate with each other making use of the capabilities of the new Arduino Connector. Arduino Create Cloud now enables users to manage individual IoT devices and program them remotely, independently from where they are located. Arduino has also revised its “out-of-the-box experience”, which enables anybody to set up a new device from scratch from the cloud without any previous knowledge by following a web based wizard. The initial release has been sponsored by Intel and supports X86/X86_64 boards. As a reference implementation, a simplified user experience has been designed for the AAEON UP² board, although other platforms are already supported by the Arduino Create Cloud platform (Intel NUC, Dell Wyse, Gigabyte GB-BXT). Arduino plans to expand support for Linux based IoT devices running on other hardware architectures.
There is no let-up in a trend that is now well-established: newly developed circuits must support higher data rates with increasingly tiny circuit dimensions, all the while consuming less power. As a consequence, development engineers are faced with major challenges and the subject of power integrity is becoming increasingly important.

Higher data rates are a driving force behind the increasing quality requirements for clock and data signals. In order to achieve lower power consumption, chipsets are now used with smaller and smaller supply voltages. The actual supply voltage must be free of interference and conform to increasingly stringent tolerance limits so that the signals generated by the chipsets can satisfy the demanding signal integrity requirements. This is why the subject of power integrity is growing in importance.

Power integrity involves ensuring a high-quality supply voltage. For electronic circuits, the relevant supply voltages are almost exclusively DC voltages. An oscilloscope with the appropriate accessories is generally used to make these quality measurements. The oscilloscope must be capable of displaying the supply voltages with high resolution and extremely low inherent noise.

Ideally, the DC supply voltages should be constant with zero noise. In reality, however, they always exhibit a certain amount of ripple and superimposed noise. Understanding why this is the case requires a look into the design of the supply voltage network.

Typically, the source of a supply voltage network (e.g. an AC/DC power supply or a battery) provides the on-board voltage. The on-board voltage is a DC voltage with common voltage levels such as 12V or 5V. This primary supply is then used to feed the necessary voltages and currents to all of the active components. However, since different components need different voltages, we might commonly encounter 10 to
20 different voltage levels. What this means for the developer is that the main on-board voltage must be adapted for every component. Highly efficient switching regulators are generally used for this purpose. One disadvantage of switching regulators compared to less efficient linear regulators is that the DC voltage is corrupted during the regulation process and periodic noise is superimposed on the DC signal. This residual noise is known as ripple.

During conversion of the voltage levels, random (nonperiodic) disturbances, which are generally categorized as noise, occur in addition to the ripple. The major contributors here are the noise of the voltage source and the noise produced by the switching currents flowing in the supplied circuit. Other relevant components include the thermal noise as well as interference from nearby circuits.

In addition to these disturbances and interference related to the switching regulation and design, we should also analyze dynamic behaviour. Sudden changes in the load current (e.g. due to a microcontroller changing state from idle to busy) can cause a momentary dip in the supply voltage. Just like the ripple and noise, this dip must not exceed the limits specified by the manufacturer, i.e. it must be regulated – return to nominal value – within an acceptable time interval.

DC accuracy is another key characteristic for voltage supplies. Here, two parameters are relevant: the absolute voltage level and the long-term stability of the voltage level. In order to ensure that all of the discussed parameters fall within the specified limits, it is important to verify these parameters using suitable T&M equipment during the development process.

**GROWING T&M CHALLENGE**

The requirements for measuring noise, ripple, dynamic behaviour and DC accuracy have increased markedly in recent years. Supply voltage levels for many components are decreasing include growing integration density on chips and the smaller dimensions needed to achieve this integration density. Naturally, there is also the design objective of lower power consumption. In parallel, the permissible tolerances for ripple and noise have also been significantly reduced by the chip manufacturers. This trend means that the interference signals that need to be measured have lower and lower levels. The technical challenge faced by the measuring system (oscilloscope and probe) is growing because the inherent noise of the measuring system is often as high as the interference signals to be measured. This noise is superimposed on the signal being measured and can make the result appear much worse than it really is. Under certain circumstances, this can cause a tolerance violation to be triggered that is not actually present (see Figure 1).

Another important issue is that an inadequate voltage offset is often set on the oscilloscope, which means the optimum vertical resolution is not fully utilized. This produces a further increase in measurement uncertainty. Possible solutions include using the oscilloscope’s AC mode or inserting a DC blocker. However, this causes the information about the DC voltage component to be lost, meaning any slow drift cannot be detected. In order to be certain – upon completion of the measurement – that the DC voltage, including any drift, ripple and noise, is within the specified tolerance, it is essential to use a high-performance measuring system.

This article continues by considering the use of frequency-domain analysis in the characterisation of power supply quality – click the panel below for full pdf.
ARE YOU CLOSE TO THE FLICKER NOISE FLOOR?

If you are working with very small signal levels, the question may arise; what is the smallest signal you can readily measure?

My first project as an engineer was to measure the settling time of what was going to be a 6½ digit DMM. It didn’t seem like a big deal, I just had to figure out the final settled value and work my way backward to the smallest detectable change: that is, the point at which the measured value stopped fluctuating. I got everything setup, shorted the inputs, and started increasing the aperture time. (In a DMM, this is the interval during which the signal gets integrated or averaged.) As expected, the noise would come down … until it didn’t. The baseline just kept moving. I had eliminated extrinsic noise sources, thermal EMF, and even draughts from the air conditioning vents. These random fluctuations were coming from the intrinsic noise of the circuit. But after eliminating most of the broadband noise, there was this other noise that would not go away. Anyone who has tried this would have noticed the same limitation. To the contrary, we may find more noise than if we had stopped sooner! We know that we are in the 1/f noise region when that happens.

This so-called 1/f noise (or flicker noise) is the most pervasive limitation for precision measurements. The name comes from the fact that its power spectral density is inversely proportional to frequency, as expressed by:

\[ \text{Noise power (f)} = \frac{k}{f^\alpha} \]

Where \( k \) is a magnitude coefficient and \( \alpha \) is an exponent that will take values greater than 0, but the canonical form is for \( \alpha = 1 \). This noise eventually becomes smaller than broadband noise, producing a corner as shown in Figure 1. Evidence of this type of noise has been found outside of electronic circuits, including in the rotation of the Earth, economic indicators, and biological systems, to name a few. While the fundamental cause keeps eluding the most brilliant scientists, we must understand how to mitigate it if we want to perform low level measurements.

Let’s start with off-the-shelf components. The highest sensitivity ADC you will find these days in an IC is AD7177-2, and that is 200 nV p-p at 5 samples/sec. But we can do better than that by adding some gain before the ADC. We need an amplifier that is both low noise and with a
low 1/f corner. The easiest is to look up the 0.1 Hz to 10 Hz noise specification on the data sheet, which is equivalent to recording measurements for 10 seconds with 10 Hz bandwidth.

You may have read about the AD797 op amp being used in the LIGO experiment to detect gravitational waves for the first time. The AD797 has a noise specification of 50 nV p-p (8 nV rms) from 0.1 Hz to 10 Hz. The AD8428, the lowest noise instrumentation amplifier, is only 40 nV p-p (7 nV rms). Because these amplifiers are built in bipolar processes, their current noise can be significant if used with large source resistance (including gain resistors), and current noise also has a 1/f corner! And don’t forget that resistors themselves can show current-dependent excess noise due to their construction. Metal foil and wirewound resistors tend to have the lowest noise indices.

A neat trick to avoid 1/f noise is to modulate the signal to a region where there is no 1/f noise and then demodulate it. This trick, known as chopper stabilization, has been used for decades to shift the 1/f noise to a different frequency band, where it can be easily filtered out. Zero-drift op amps like the ADA4528-1 and ADA4522-1 take advantage of this (and other tricks) to get about 100 nV p-p (16 nV rms) from 0.1 Hz to 10 Hz, mostly due to white noise. A simpler alternative is to parallel multiple amplifiers to reach lower noise levels, since this is equivalent to averaging uncorrelated noise sources.

The bottom line is that with off-the-shelf components, you can detect signals just below the 10 nV mark, and paralleling amplifiers will get you close to the 1 nV level. Anything below that will require special (and perhaps pricey) techniques. But no matter what you do, 1/f will always find a way to resurface.

So, what if we were to record several measurements for a really long time? Would 1/f noise make this an impossible task? Let us bring some perspective: if we had recorded the AD797 noise from the moment of the Big Bang until the time of reading this article (using the assumption that the elapsed time is 4.32 x 10^{17} seconds) it would only be three times larger than if we had measured it for the last 10 seconds. (That is somewhat hypothetical, since there is no evidence 1/f follows this curve for that long. Ageing and other factors start to play in at longer measurement intervals.)

REFERENCES

Gustavo Castro is a system applications engineer in the Linear and Precision Technology Group in Wilmington, Massachusetts. His main interests are analogue and mixed-signal design for precision signal conditioning and electronic instrumentation. Prior to joining Analog Devices in 2011, he worked for 10 years designing high performance digital multimeters and precision DC sources at National Instruments.
HIGH POWER DENSITY SYSTEMS DEMAND HIGH CURRENT CONVERTERS

By Steve Knoth, Linear Technology

The expanding market for high current, low voltage digital ICs reached $9.2B in 2016 [source: Intense Research Co]. This group of digital ICs includes microcontrollers and microprocessors (µC & µP), programmable logic devices (PLDs), digital signal processors (DSPs), application specific integrated circuit (ASICs), programmable logic devices (PLDs) and graphics processor units (GPUs). Furthermore, looking at the projections for a big subset of this market – Field Programmable Gate Array ICs (FPGAs) – this segment was valued at $3.92B in 2014 and is expected to reach $7.23B by 2022, with a CAGR of 7.41% between 2016 and 2022 [source: market-sandmarkets.com]. High power density digital ICs have penetrated into virtually every embedded system. These systems include, but are not limited to, industrial, communications, telecom, servers, medical, gaming, consumer audio/video and automotive. FPGAs are enabling cutting-edge applications to come to fruition within these market segments, for example in automotive applications to remove human errors, such as advanced driver assistance systems (ADAS) and collision avoidance systems. Government–mandated safety features such as anti-lock brake systems, stability control and electronically controlled independent suspension systems have necessitated the use of FPGAs. In the consumer electronics sector, the demand for Internet of things (IoT), machine to machine (M2M) and the growth of data and server centres driven by the demands of large data storage and cloud computing are some of the factors also driving the FPGA market.

SWITCHING REGULATORS VS CHARGE PUMPS & LDOS

These high power density digital IC-based systems have a unique set of power requirements. The combination of high current, low voltage and fast transient response for this current generation of FPGA and ASIC processors place ever more stringent demands on the supplies that power the device. These digital ICs are powerful, yet temperamental from a power standpoint. Traditionally, efficient switching regulator controllers with separate high power MOSFETs have been used to power these devices but they have exhibited potential noise interference issues, slower transient response and layout limitations. As a result, in recent years low dropout regulators (LDOs) that minimize heat have been used as an alternative, but are not without their own set of limitations. However, thanks to recent product innovations in this area, the trend is changing. Newer high power monolithic switching regulators no longer come with performance tradeoffs and are rapidly finding their way into these applications.

Low voltage high current step-down conversion and regulation can be achieved via a variety of methods with a variety of design tradeoffs. Switching regulator controllers operate with high efficiency for high currents over a wide range of voltages but require external components such as inductors and capacitors (and FETs in the controller case) for operation. Inductorless charge pumps (or switched capacitor voltage converters) can also be used to achieve lower voltage conversion but are limited in output current capability, suffer from poor transient performance and require more external components versus a linear regulator. As a result, charge pumps are not commonly found in digital IC power applications. Conversely, linear regulators and especially LDOs are simple in that they only require two external capacitors to operate. However, they may be power limited depending on the size of the input-to-output voltage differential across the IC and how much current is demanded by the load, plus the thermal resistance characteristics of the package. This limits their penetration into powering digital ICs.

HIGH CURRENT MONOLITHIC BUCK CONVERTER DESIGN CHALLENGES

Closely following Moore’s Law (originally conceived in 1965), wafer fabrication technology line widths are ever decreasing, therefore requiring lower voltage operation of digital ICs. Smaller geometry processes allow higher integration of more power-hungry features in the end product.
For example, modern computer servers and communication routing systems demand higher bandwidth to process more computing data and internet traffic. Cars have more on-board electronics for entertainment, navigation, self-driving features, and even engine control. As a result, system current consumption and associated total power required increases. Therefore state of the art packaging and innovative internal power stage design are required to take the heat out of the power IC while delivering unprecedented power. The requirements for high power supply rejection (PSRR) and low output voltage noise or ripple are two additional challenges which also need consideration. A device with high supply rejection can more easily filter and reject noise at the input, resulting in a clean and stable output. Further, a device with low output voltage noise across a wide bandwidth or low output ripple is beneficial to power today’s modern low-noise rails where noise sensitivity is a major design consideration. As the speed requirements for high end FPGAs increase, the supply noise tolerance continues to decrease in order to minimize bit errors. These noise-induced digital faults drastically reduce the effective data throughput speeds for these high speed PLDs. Input supply noise at high currents is clearly an important but demanding specification. Higher transceiver speeds – in FPGAs for example - dictate higher current levels due to higher power consumption from fine-geometry circuit switching. These ICs are fast – they may cycle load current from near zero to several amps in tens to hundreds of nanoseconds, requiring a regulator with ultrafast transient response. With board area reserved for the power regulators ever decreasing, it is well known that a monolithic switching regulator with fast switching frequency reduces the size of external components and therefore total solution size, with a tradeoff of some minor loss in efficiency due to switching losses at higher frequencies. However, a new generation of monolithic switching regulators provides unique features that significantly reduce the amount of switching losses even at higher frequencies. Namely, synchronous operation with integrated high and low side switches allows for better control of their gate voltages which greatly reduces dead-time thereby resulting in higher efficiency operation.

NEW HIGH CURRENT BUCK CONVERTERS
One of the biggest challenges with high current monolithic switchers is their ability to dissipate heat resulting from significant power loss in the IC. This challenge is met by using thermally enhanced ball-grid array (BGA) packages where the majority of the solder balls are dedicated for power pins (VIN, SW, GND), such that the heat can be easily transferred from the IC into the board. Large copper planes on the board connecting to these power pins allows for the heat to spread more evenly. It is clear that a buck converter solution which solves the issues outlined above needs to have the following attributes:

- Fast switching frequency – reduces size of external components
- Zero dead-time design - for increased efficiency
- Monolithic – onboard power devices for smaller solution size
- Synchronous operation – higher efficiency and reduced power loss
- Simple design - minimal external components required
- Very low output ripple
- Fast transient response time
- Operation over a wide input/output voltage range
- High output current capability
- Excellent thermal performance
- Compact footprint

This article continues by detailing the characteristics of a high-integration device intended to meet this list of requirements, and follows it with typical circuit configurations - click the panel below.
The Common Weakness Enumeration (CWE) and the Common Quality Enumeration (CQE) represent efforts for identifying and classifying software-security issues. Given the increased interest in security and safety development, it’s surprising how few know about the Common Weakness Enumeration (CWE) and the Common Quality Enumeration (CQE). Both are industry projects hosted by MITRE.

CWE is a community-developed list of common software security weaknesses such as buffer overflow. It’s designed to be a baseline for “weakness identification, mitigation, and prevention efforts.”

“The Common Quality Enumeration (CQE) project is developing a “lingua-franca” of software quality issues aimed at getting tool creators to adopt a common identification system—allowing them to define quality issues easily and ultimately create better software.” The two are complementary and every programmer should be aware of their contents.

COMMON WEAKNESS ENUMERATION (CWE)
All software developers should take a look at CWE, as it serves as a common language for describing software security weaknesses in architecture, design, or code. It can also be used to measure software security tools from programming languages to static-analysis tools that target the weaknesses. It also addresses weaknesses in identification, mitigation, and prevention efforts.

Some common software weaknesses enumerated by CWE include buffer overflows, structure and validity problems, common special element manipulations, channel and path errors, handler errors, user interface errors, path-name traversal and equivalence errors, authentication errors, resource-management errors, insufficient verification of data, code evaluation and injection, and randomness and predictability.

CWE is based on work that MITRE began in 1999 called the Common Vulnerabilities and Exposures (CVE). The CVE list was a preliminary classification and categorization of vulnerabilities, attacks, faults, and other concepts to help define common software weaknesses.

The CWE List is numbered and detailed. For example, CWE-121 is Stack-based Buffer Overflow (see Figure). A variety of other buffer overflow entries are in the mix as well. Included are a description, relationship links to other entries, applicable platforms such as C and C++, common consequences, examples, and mitigations.

Quite a few items are listed, so there are different views, or collections, that provide more targeted lists, such as the one for C applications. This is a list of 79 items, although others can be applicable to C applications. This list includes the primary ones, and has items such as buffer overflows, conversion errors, and pointer issues.

Some languages such as Ada, SPARK and Rust address many of the items in the list, while tools such as static- and dynamic-analysis tools can be used as well.

COMMON QUALITY ENUMERATION (CQE)
Programmers want to deliver quality code, but what does that really mean? Part of the challenge is coming up with a common set of descriptions and then enumerating and addressing details. CQE is a work in progress.

MITRE’s John Marien notes, “The Common Weakness Enumeration (CWE) lists quality
### CWE-121: Stack-based Buffer Overflow

<table>
<thead>
<tr>
<th>Weakness ID: 121</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abstraction: Variant</td>
</tr>
<tr>
<td>Structure: Simple</td>
</tr>
</tbody>
</table>

**Presentation Filter:** Basic

**Description**
A stack-based buffer overflow condition is a condition where the buffer being overwritten is a parameter to a function.

**Relationships**
The table below shows the weaknesses and high level categories that are related: ParentOf, MemberOf and give insight to similar items that may exist at higher and lower levels. PeerOf and CanAlsoBe are defined to show similar weaknesses that the user may want to consider.

- **Relevant to the view** "Research Concepts" (CWE-1000)
- **Relevant to the view** "Development Concepts" (CWE-699)

**Modes Of Introduction**
The different Modes of Introduction provide information about how and when this weakness may occur, while the Note provides a typical example.

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Figure 1. CWE entries like this, on buffer overflow, include standard sections such as the description, relationship links to other entries, applicable platforms such as C and C++, common consequences, examples and mitigations.

A large number of software tools and programming languages are designed to improve code quality. No one language or tool addresses all quality issues or application areas. Many overlapping tools make the discussion of quality difficult. Coming up with a common discussion language and then collecting information about quality issues and solutions could be used for a competitive advantage.

"MITRE is helming [steering] the CQE project because automated-tool creators trust us with proprietary data they would not share with each other," says Marien. «They know we won’t use it for a competitive advantage."

Hopefully the CQE lingua-franca will be widely adopted. This could not come too soon. CWE is useful now, and CQE is on its way.

William Wong is Technical Editor at Electronic-Design.com, where this article first appeared.
Getting proper data-acquisition and measurement results may be a matter of “timing it right.” In life, it seems like you’re always either doing the wrong thing at the right time, or the right thing at the wrong time. So why don’t we take this experience into account when we acquire data or make measurements? After all, it can be a real problem if you only record what happens and not when it happens.

Consider a noisy signal channel. It’s obvious that you run the risk of getting a somewhat “wrong” measurement, as in one that has an error due to the measurement noise. We know we might get the wrong thing, but we usually assume we’ll get it at the right time; i.e., the time we wanted. But there’s another significant source of noise in a data-acquisition channel. You may not have sampled that signal at the “right” time. And therefore, you might have got the right thing at the wrong time.

Too often, I see measurement systems designed with an obsession on getting the right thing, but with scant attention taken to ensure that it was got at the right time. It’s hard to convince people that “time noise” can sometimes be as much of an issue as “amplitude noise.” Practically all post-processing of sampled data is predicated on the signal having been uniformly sampled. This crucial element is often mentioned just once, in one of the boring early chapters of the Signal Processing textbook that today’s impatient young engineers are keen to move on from. So, cut this out and stick it inside the front cover of your textbook:

You can’t filter or transform a set of measurements unless you know when they were measured. A data point $y(t)$ is a point on a plane with coordinates $(t,y)$ and you do not have full information about that point and its influence unless you know both $t$ and $y$.

The obvious way to address this is to time-stamp all your measurements. I had that drilled into me as a young engineer. Every time you measure something, write down the time when you measured it. The result, after a sequence of measurements, is a proper $(t,y)$ dataset. It doesn’t matter too much if you don’t take your readings at constant intervals. There are interpolation techniques that do a good job of reconstructing an underlying implied continuous process (a voltage, a temperature, a carrier frequency, anything really) from data points separated by known irregular intervals. If the irregularity of the measurement issues is unknown, of course, it’s another matter entirely.

POINTS OF UNCERTAINTY
The killer assumption we make too often is that when we set up some kind of sampling system (for example, using an ADC), we just connect some sort of sampling clock. And hey, presto, we’ll get a dataset of uniformly sampled data points, spaced in time by a known interval. But with any real clock, the frequency is never quite constant, and so the interval between sampling points is also slightly variable.
This isn’t a problem that goes away suddenly when the uncertainty of your measurement timing is reduced below a certain threshold. The clocks used to time the acquisition or reconstruction of signals between analogue and digital domains will often suffer from a certain amount of jitter—an inconsistency in the position of the edges of the clock signal. The mean frequency of the clock may be correct, but each edge may be located a small, unknowable distance away from the “ideal” position.

You can think of this uncertainty in edge timing as being the result of phase modulation by some otherwise unknowable signal. Modulation in the time domain has an impact in the frequency domain. Spectral analysis (e.g., taking a fast Fourier transform, or FFT) of an ideal clock’s fundamental component should show up as a single frequency value—a nice sharp line in the FFT. But if the clock’s edges are moving in time, additional sideband frequencies are generated. This smears out the sharp fundamental into a broader spectrum.

But why is this a problem in a “digital” system? Why should the frequency spectrum of a clock have any impact on the performance of a system using that clock?

Here’s a concrete example. I wanted to assess the impact of various clock-generation methodologies on audio reproduction as part of a project to build a multichannel interface for PDM (pulse density modulation) microphones. These microphones contain a delta-sigma modulator front end that spits out a one-bit stream clocked with an incoming clock from the interface. That one-bit stream is heavily decimated in the interface to filter off the high-frequency noise inherent in the ADC, leaving nice multibit audio at a more conventional sample rate. Standard stuff.

Here’s the important bit: Anything that modulates the clock, modulates the output data in essentially the same way. If the clock used by the ADC is smeared out in frequency, the data that comes out of the system will inherit that smearing. That’s because when it is reproduced, or analyzed by an FFT, the time information in the wobbly clock edges that caused the smearing will be unavailable; therefore, they can’t be taken into account. Even though we’re talking about clock edges that might be in the wrong place by only a fraction of a nanosecond here and there, the mismatch between where sampling actually happened and where you assume it happened without the \textit{a priori} information is enough to mess things up in the data.

If this seems a bit remote to you, consider this: Sometimes all of the information in a signal is in the time domain, and none is in the amplitude domain. It has long been known, for example, that much of the information in a complex, bandlimited signal such as speech can be extracted from knowledge only of the positions in time of the zero crossings. In that case, we get a set of data points \((t,0)\) with no amplitude content at all. Yet it’s usually pretty intelligible. Other examples are binary PDM and PWM—pulse-density modulated and pulse-width modulated—signals. These signals are processed in such a way that the value of the “1” and “0” state voltages don’t contribute to the reconstructed signal. The information is contained in the duty cycle of the binary stream.

**EYEBALLING IT**

![Figure 1. The 2.822-MHz (nominal) clock from a crystal-referenced FLL.](image-url)
Let’s go graphical. Figures 1 and 2 show spectral analyses of two versions of a 2.822-MHz clock intended to feed a PDM microphone interface on a Cypress PSoC 6. PDM technology now dominates the consumer audio microphone space. These were captured on a venerable Hewlett-Packard (now Keysight) 89410A, a now-obsolete but much-loved workhorse of my testbench for over 20 years. If you like tight, sharply defined spectral lines, it’s not hard to choose.

The clock of Figure 1 was derived from a fast-starting, low-power frequency-locked loop (FLL), while Fig. 2 shows the spectrum of the system phase-locked loop (PLL). That block takes a little longer to start up and consumes a little more power. Both of them were driven by a reference frequency sourced from the system crystal oscillator, running with my favourite audio crystal frequency of 17.2032 MHz (available from my favourite crystal supplier IQD, as the LFXTAL063075).

Now jump to Figures 3 and 4. For this test, I used the PDM emulation hardware in an Audio Precision APx525. When stimulated by the applied clock, the PDM interface produces a one-bit signal modulated by your choice of test signal, in this case a 1-kHz sinewave at −20 dBFS (okay, call me old-fashioned). The plots show the spectrum from 0.9 to 1.1 kHz; I suspect a little bug in the axis marking routine...

So, no prizes for guessing which plot of the audio result is associated with each plot of the clock’s spectral makeup. Fig. 4 is nice. Fig. 3 would get you kicked out of any audio-savvy company. And there are non-audio measurements requiring this level of cleanliness, too. If you’re looking for closely spaced vibrational modes in stiff structures, you don’t want the ADCs that are converting your accelerometer signals to be hampered by...
bad clocks like this. You’ll get this effect with whatever architecture of ADC you use. It’s not just a delta-sigma or one-bit thing.

There was never any real danger that we would use the low-quality clock of Fig. 1 in our solution. Not on my watch (maybe in my watch, but that’s a low-power microphone discussion for another day). Rather, I felt it was important to make these measurements, to show the less-experienced and the sceptical amongst my colleagues that, when it comes to audio, you can’t cut corners with clocking.

Have you had a hard-to-find performance problem that turned out to be down to clock spectral quality?

Kendall Castor-Perry is Senior MTS Architect, Programmable Systems Division, Cypress Semiconductor

For nearly four decades, Kendall Castor-Perry has been chasing signals through electronic systems, wringing out the information they are hiding. He’s a world-class authority on filters and precision analog circuit engineering and a tireless champion of the needs of the customer. He has been widely published and syndicated, especially when sharing his extensive filtering knowledge as “The Filter Wizard.” He holds a BA in Physics from Oxford and an MBA in MBA stuff from London Business School. Kendall is currently Senior MTS Architect in Cypress Semiconductor’s Programmable Systems Division, pushing on the performance:power:price boundaries constraining tomorrow’s critical sensor-processing systems.

This article first appeared at ElectronicDesign.com
Embedded systems are experiencing rapid growth in both existing markets and within developing markets, with analysts predicting the embedded system market will be worth $225 billion by 2021 (source; Ref 1). This growth is driven by the continued development of several key industry megatrends including Internet of Things (IoT) and Industrial Internet of Things (IIoT), Industry 4.0 and Cyber Physical Systems, along with the proliferation of vision enabled systems at the edge.

Many of these applications require the deployment of high performance systems “at the edge”. For applications with a large number of deployments, the recurring engineering cost of the solution is of critical importance and will determine the viability of the solution.

One driving factor in the reduction of the recurring engineering costs is implementing tighter system integration, including component integration. A typical embedded system contains components including processors, digital logic, interfacing, volatile and non-volatile memory, mixed signal components, sensors and supporting elements such as clocking and power supplies. Tighter integration also enables reduced complexity and therefore reduced costs in the printed circuit board and its assembly.

Devices that are programmable at a number of levels can provide not only the performance required, but also enable tighter system integration to be realised. Xilinx uses the terminology “All Programmable” to indicate that its devices in this class have programmability in the ability to configure their programmable logic aspects; in software programming of embedded processor cores; and in configuration of function-specific embedded blocks. Devices such as Field Programmable Gate Arrays (FPGA) and heterogeneous System on Chips (SoCs) from the company's cost-optimised portfolio are tailored for different application demands.

Applications that are I/O intensive can be served by the Spartan-6 and Spartan-7 families, that are I/O Optimised. Oriented to applications characterised by a need for high throughput via transceivers, the Artix family offers gigabit transceivers. Zynq-7000 SoCs with dual core Arm Cortex-A9 and single core Cortex-A9 as “hard” blocks are designated as system-optimised. The portfolio addresses applications from cloud computing and image processing, to sensor fusion, precision control and safety and security.

Using this suite of devices, it is possible to create a tighter integrated system in a number of ways. Processor integration combines processor and digital logic within the same device. This can be achieved using the MicroBlaze softcore 32-bit processor (which is configured within the programmable logic array) or the Zynq-7000 Cortex-A9 cores.

Mixed signal integration makes use of the analogue capabilities within 7-series devices.
An analogue/mixed signal module termed XADC provides dual 1 MSPS ADCs capable of internally multiplexing between 17 differential inputs. To provide DAC capabilities, pulse width modulation can be used, while for higher sampling rates, delta sigma techniques can be implemented, employing the differential capabilities of the IO cells.

Interface simplification: programmable logic provides the ability to implement any-to-any interfacing, thanks to the wide range of standards supported directly by the IO structures. Coupled with the ability to implement protocol functions within the programmable logic, this allows legacy, bespoke and standard interfaces to be implemented. This flexibility also enables the reduction of discrete PHY devices required, for instance HDMI or MIPI DPHY.

In the case of memory architecture, applying a unified approach enables significant simplification. It is possible to store the application software and FPGA bitstream within the same non-volatile memory. Volatile memory such as DDR can also be shared between the processor and the FPGA application.

Simplification of clocking architecture is aided as integration within a single device removes the need for separate oscillators for the digital logic and processors, while clocking management tiles, provision of phase locked loops (PLL) and mixed-mode clock managers (MMCM), can be used to generate additional system clocks, and provide the ability for agile output frequency and phase adjustment.

Development of these integrated applications can also make use of a range of IP cores provided as library elements within the devices’ development environment, Vivado. For algorithmic and image- or signal-processing applications, high-level synthesis can be used to define the functionality using a high-level language such as C or C++, reducing the overall development time.

**INTEGRATION EXAMPLE**

IIoT and cyber physical systems often contain embedded vision systems, motor or actuation control, and wired or wireless interconnectivity, along with location and environmental sensors. A traditional non-integrated solution would use a processor to perform the high-level decision making and communications, and an FPGA to perform the sensor interfacing, image processing pipeline and resultant motor or actuator control.

This solution along with an increased number of components also brings a more complicated clocking and power architecture contributing towards the recurring engineering cost.

*This article concludes by outlining further application scenarios in which the use of high-integration parts can simplify the final PCB; click the panel below.*
Automotive LED lighting controller drives external MOSFET

Texas Instruments (TI) has developed what it believes to be the first 3-channel high-side linear automotive light-emitting diode (LED) controller without internal MOSFETs; the TPS92830-Q1 LED controller gives designers the freedom to select the best MOSFET for their system requirements. An on-chip pulse-width modulation (PWM) generator or PWM input enables flexible dimming. Designers can use either the analogue control or PWM to manage an output current of more than 150 mA per channel, to power automotive rear combination lamps and daytime running lights.

Biosensors with ECG function for HRM in wearables

Silicon Labs has introduced a family of optical biometric sensors providing advanced heart rate monitoring (HRM) by transcutaneous optical measurements, along with electrocardiogram (ECG) capabilities, for a range of wearable fitness and wellness products. Si117x sensor modules combine ultra-low power, high sensitivity and integration, for smart watches and wrist-based, patch-type and other wearables requiring long battery life and enhanced HRM accuracy. To simplify development and speed time to market, Silicon Labs offers a complete, end-to-end sensing solution.

25V n-channel power MOSFET has 0.58 mΩ on-resistance

Vishay Intertechnology has added a 25V n-channel TrenchFET Gen IV power MOSFET that claims the lowest maximum on-resistance for such a device: 0.58 mΩ at 10V. The Vishay Siliconix SiRA20DP offers the lowest gate charge and gate charge times on-resistance figure of merit (FOM) for devices with on-resistance below 0.6 mΩ. It features low gate charge of 61 nC and is packaged in a 6 by 5 mm PowerPAK SO-8 single package. The device offers a 32% lower FOM (than competitors) of 0.035 Ω*nC; all other 25V n-channel MOSFETs feature on-resistance that is 11% higher or more.

Micro-display for VR and AR wearable products

Specialist distributor Framos (Munich, Germany) has Sony Semiconductor’s ECX335B OLED Micro Display; a super-small, thin, lightweight and fast device intended for virtual-reality and augmented-reality wearable products. The ECX335B Organic Light-Emitting Diode Microdisplay is suited for head-mounted devices, in which it provides lightweight and fast response speed. The ECX335B is a small 0.71 inch (1.8cm) diagonal active matrix colour OLED panel module based on single crystal silicon substrate and provides a Full-HD RGB resolution of 1920 x 1080 dots.
Maxim aims for clinical-grade vital signs monitoring with pulse sensor/AFE chips

Maxim Integrated has introduced two devices for the medical monitoring and fitness wearables sector; an optical pulse oximeter/heart rate sensor IC; and an ECG/biosigns analogue front end (AFE). With both, Maxim says it has improved in power (battery life), accuracy and size (small form factor) over prior offerings. MAX30001 is a complete, biopotential and bioimpedance (BioZ), AFE for wearables. It has two channels; a bioimpedance (skin resistance) channel that has an excitation current source and voltage measurement connection; and an ECG input that measures the body’s own potentials. MAX86140 and MAX86141 are sensor chips that can be used to measure PPG (photo-plethysmography) signals on the wrist, finger, and ear to detect heart rate, heart rate variability, and pulse oximetry. In common with other such sensor devices, the ICs drive multiple LEDs (three channels, up to six LEDs) of different wavelengths and detect blood flow through the skin.

Microchip security IC comes with 3rd-party & cloud services

A package announced by Microchip aims to assist designers to protect their IP, and deploy secured connected systems, with its “CryptoAuthentication” device; and a Security Design Partner Programme. Hardware is in the form of the ATECC608A CryptoAuthentication device, a secure element that allows developers to add hardware-based security to their designs, to create, protect and authenticate a device’s unique and trusted identity. OEMs also have access to Microchip’s Security Design Partner Programme including Amazon Web Services (AWS) and Google Cloud Platform.

24:1 stepdown IC yields logic-level rails from 48V

This step-down power supply IC from Rohm is aimed at 48V automotive systems; its “Nano Pulse” control approach achieves a step-down ratio of 24:1 between input and output voltages. BD9V100MUF-C is a DC/DC converter with built-in MOSFET that can generate output voltages of 3.3V or 5V (minimum 2.5V at max input) from input voltages up to 60V at a switching frequency of 2 MHz. The chip minimum ON time switching of 9 nsec, for single-stage voltage conversion in 48 V systems such as those used in mild hybrid vehicles. At 2 MHz the number of parts required is halved.

Digitisers plus Nvidia GPUs enable fast signal processing

Spectrum Instrumentation has developed a software package that bridges its signal-capture digitisers with graphical processors using Nvidia’s CUDA architecture. The combination implements GPGPU – general purpose computing on graphical processing units – to provide high-speed, highly-parallel signal processing without the need for either extremely powerful conventional host processors, or for custom programming of FPGAs. The software maps the inherent parallelism of DSP functions – that is, similar operations applied to many samples – to the many-core structure of the GPU, originally designed for pixel processing.
Tek adds deep analysis options to mixed-signal scope range

Making use of the touch interface and 12-bit resolution of its 5 Series MSOs, Tektronix has added measurement options that include power analysis, Automotive Ethernet testing, and serial trigger and decode for the aerospace and automotive markets. These options exploit 5 Series MSO features features that also include up to 8 input channels and large high-definition capacitive touch display with intuitive Direct Access user interface. Also added to Tek's scope range are 5 Series MSO low profile (display-less) formats for advanced research and manufacturing applications.

Active FET-based-rectifier controller with reverse protection

LT8672 is an active rectifier controller with reverse input protection to –40V. The device’s 3V to 42V input voltage capability is suitable for automotive applications which must regulate through cold-crank and stop-start scenarios with minimum input voltages as low as 3.0V and load dump transients up to 40V. The LT8672 drives an external N-channel MOSFET, offering a 20 mV drop, eliminating requirements for a heat sink. Its ultrafast transient response enables it to meet stringent automotive applications requiring AC input ripple rectification up to 100 kHz.

Debug support for RISC-V core IP and silicon

Development tool vendor Lauterbach, and SiFive, fabless provider of customised, open-source-enabled semiconductors, have announced that Lauterbach’s TRACE32 toolset will provide debug capabilities for SiFive’s E31 and E51 RISC-V Core IP, based on the free and open RISC-V ISA. This architecture joins products from more than 75 silicon companies supported by Lauterbach’s TRACE32 debug tools that promise to aid development of robust code whilst minimising time lost to debugging. Lauterbach TRACE32 provides multicore debugging on individual hardware threads of SiFive cores, enabling debugging right from the reset vector, which analyses startup codes and other key functions. Lauterbach also provides high-level and assembler debugging for a variety of standard ISA extensions, such as compressed instructions and floating point. It also fully supports the JTAG Debug Transport Module (DTM) in all SiFive chips.

Micro infrared imager, now in distribution

Distributor and thermal imaging source Acal Bfi has FLIR’s Lepton 3 micro-camera that offers IR imaging performance in an ultra-compact package. Lepton is a complete long-wave infrared (LWIR) camera module designed to interface easily into native mobile-device interfaces and other consumer electronics, using a standard SPI video or two-wire I2C serial control interface. Multiple proprietary technologies, including wafer-level detector packaging and micro-optics, are packed into the single, low-power chip which measures 11.8 x 12.7 x 7.2 mm, or less, depending on model.
Aluminium electrolytic capacitor breaks energy density barriers

Cornell Dubilier’s THA and THAS Series Thinpack capacitors claim the highest-energy density available in low-profile aluminium electrolytic technology. The company quotes dimensions of 8.2 mm, and 9 mm, thick, respectively, for the 85ºC THA Series and 105ºC THAS Series Thinpack capacitors. This is comparable in height to V-chip electrolytics, tantalums and board-mounted axials, yet offering much higher bulk-storage energy density. A single THA/THAS capacitor can replace an array of SMT, axial or radial aluminium electrolytic or solid tantalum capacitance arrays.

High-accuracy digital temperature sensor IC

Sensirion’s STS35 temperature sensor is the most accurate sensor the company has produced in the STS3x series, intended for markets such as the medical (body temperature measurement) and automotive sectors. With accuracy of ΔT = ± 0.1°C, the sensor’s function set includes enhanced signal processing, two distinct and user-selectable I2C addresses and communication speeds of up to 1 MHz. The DFN package measures 2.5 x 2.5 x 0.9 mm and its supply voltage range is 2.4 V to 5.5 V. The STS35 includes a configurable alert function, allowing it to be used as a temperature watchdog.

Single-package, 5-output voltage regulator

Infineon’s IRPS5401 is a five output Point of Load (POL) digital voltage regulator for FPGAs, ASICs, and other multi-rail power systems. The IRPS5401 has been developed as a fully integrated PMIC solution that replaces multiple regulators with a single device in a 7 x 7 mm 56 pin QFN package, for single rail operation ranging from 5V to 12V, where most PMICs are only 5V. It has one 500 mA LDO output, and four configurable switching regulator outputs, two at 2A, and two at 4A. The outputs of the IRPS5401 can be used to provide the typical rails required for core, memory, and I/O voltages. The voltage output range is between 0.5 and 3.6V for regulators A to D, and between 0.25 and 5.1V for the LDO.

Single-chip radio software bridges Bluetooth and Zigbee

Silicon Labs’ multiprotocol wireless software has been designed in response to application needs for both Bluetooth (essentially, providing smartphone control-compatibility) and Zigbee – widely adopted in mesh networking and control schemes. The software expands Zigbee mesh networking with Bluetooth Beaconing and direct connectivity through smartphone apps. The approach is described as “dynamic multiprotocol” that is, using a single radio, it time-slices sessions of Bluetooth and Zigbee signalling, enabling communication with both standards. Relying in part on the inherent robustness of the Zigbee protocol, with its short packets and ability to re-try messages: and the deterministic aspects of Bluetooth, Silicon Labs says it has extensively verified that real-world connection scenarios maintain connectivity without problems.
Editor’s note; Canonical is the body, and operating company, behind the open-source, Linux-variant, operating system Ubuntu. At this season, many bodies offer their predictions for the coming year: Canonical and its Vice President got in ahead of the pack, so we will share the their thoughts here…

“We are seeing the shift in IoT deployments from the proof-of-concept stage into production, as more enterprises are starting to successfully navigate the challenge of ROI for their projects. This is demonstrated by the Forrester research, which revealed that 28% of enterprise organisations are now planning to adopt IoT solutions, up from 19% in 2016. These rising rates are being driven by the plummeting price of hardware components making it cheaper to deploy, while the proliferation of IoT use cases will give other businesses more impetus to make the leap themselves especially if their competitors are seen to be ahead of the game. Below are three IoT trends I expect we’ll see more of in 2018:

New use of integrated technologies; Blockchain and machine learning are the most fascinating areas for IoT innovation. Blockchain will prove particularly useful for the handling of payments and guaranteeing the integrity of transactions. With machine learning, we won’t see this move entirely to the edge of the network, but in some cases it makes a lot of sense. For example, with video surveillance in the retail environment it can be used to spot behavioural patterns of would-be shoplifters, without streaming data or personal data to the cloud. We’ll also see greater use of low power wide area networking (LPWAN) technologies, which can run unwired for long periods of time using very little power. This really proves its worth in environments where standard cellular connectivity can be intermittent, like a basement equipment room for example. LPWAN has better range and penetration of hard to reach locations, so opens up interesting use cases for heartbeat monitoring of critical equipment.

New business models; As IoT grows, connectivity embedded within products will increasingly disrupt the idea of ownership – with connected autonomous cars, for instance, consumers buy the journey, not the car. We’re moving towards outcomes over assets, consumption over capital investment. This will go way beyond cars, potentially incorporating a whole range of products. By including sensors within almost any asset, manufacturers can sense when a product is about to wear out and replace with a new one. According to Thomson Reuters, this ‘predictive maintenance’ market is expected to grow seven-fold by 2022. The IoT is enabling organisations to move to more subscription-based business models, where the sale of the asset is split between hardware and value-added services. If manufacturers can finance the asset over a longer period, they can almost remove the purchase price altogether. With investment being squeezed across the board, we’ll see these new business models adopted, removing the capital outlay friction and making the business case easier.

Security, security, security; Unfortunately, security continues to dominate the headlines for all the wrong reasons. If you look at IoT in an industrial context, the average asset life can be anything from 7-10 years (or longer!), so the ability to keep these assets updated and secure is paramount. The majority of industrial vendors are now building cloud-based services, so IoT security will remain key for both IoT adoption and driving new requirements from customers. In the consumer space it’s staggering just how many manufacturers have no security strategy regarding patching of devices against new vulnerabilities. I expect to see at least another 2-3 large scale botnet attacks on IoT related hardware in
IOT

2018 alone. This will now force a change, with brands who may have previously sold products based on getting new features to market as quickly as possible now making security a priority. Companies understand that any security backlash could torpedo their business, so it can no longer be neglected. We’ll also see a move towards consumer devices receiving security updates automatically, with little choice given to the end-user. These updates will pose minimal consumer disruption, in some cases even without the need for a device reboot. Within enterprise, we’ll see the government considering regulations preventing the purchase of devices that do not have a security strategy in place. This is something that is already being proposed by a bipartisan group of U.S. senators on who plan to introduce legislation seeking to address vulnerabilities in computing devices embedded in everyday objects.

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