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Uncommon Market: Smart grids and IoT convergence turns more data into cash
While the smart grid sensor market is set to double in size by 2014, growing to well over $200 million of annual revenue by 2018 according to IMS Research, it only represents a fraction of the global market for M2M data collection, aggregation and actuation devices.

Version control in EDA for optimum hardware design
Timing closure highlights the challenges of 45nm silicon design and below
Modeling skew requirements for interfacing protocol signals in an SoC

Predictive modeling approach boosts the development of thin-film organic electronics
Imec (Belgium), University of Bologna (Italy) and University of Mons (Belgium) have developed a unique multi-scale methodology to model the development cycle for thin-film organic electronic materials and devices.

A new class of flexible semiconductors enters the market
Printed electronics opens up large flexible sensor design opportunities
Compared to traditional electronic solutions, printed electronics offers several differentiating factors which make them particularly well suited to sensing application.

Efficient geolocation using swarm radio

The FIND-iT is a PC and Android smartphone or tablet solution that enables users to associate passive UHF radio frequency identification tags with items, as well as create inventory lists and find those objects using an Android smartphone or tablet. Three such kits are for grab.
Smart grids and IoT convergence turns more data into cash

By Julien Happich

WHILE THE SMART GRID SENSOR market is set to double in size by 2014, growing to well over $200 million of annual revenue by 2018 according to IMS Research, it only represents a fraction of the global market for M2M data collection, aggregation and actuation devices. According to a recent analysis by Machina Research, machine-to-machine communications already account for 2 billion M2M connections today and are set to grow to 18 billion in 2022, that at an incredible CAGR of 22%.

Visiting the Smart Grid Congress in Paris last month, more than hardware metering solutions, one could immediately notice the strong emphasis on data management, analysis and data monetizing opportunities. While utility providers had some metering solutions on display, like the Linky smart meter from ERDF and various smart plugs that provide power consumption data from any appliance connected through them, the congress’ biggest focus really was on how to make the best use of data through simple user interfaces. Utility providers want all the data, but end-users would most probably be offered subsets of metering data with simplified response scenarios and financial incentives to manoeuvre them into particular energy-spending habits.

Already rolling out, ERDF’s Linky.

Fluvia’s optical reader allows the company to extract power consumption information and to perform data analytics from old electricity meters.

Examples of housing environment dash boards as proposed by the TBH Alliance.
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of-Things (IoT) where M2M communications are key and often transit via the cloud.

Ijenko’s cloud-based energy management solution allows third parties (utilities, telcos, and service aggregators) to deploy their software and offer energy efficiency and demand response services to their residential consumers. This helps utilities optimize the balance between demand, micro-generation and storage (including the use of smart hybrid cars as backup energy storage).

Looking at defining the most appropriate and intuitive user interfaces for end-users to consume the energy-related data, the company co-finances the Modelec project from utility provider Direct Energie (formerly Groupe Poweo Direct Energie).

The project includes a trial with 2000 customers equipped for half of them with the Linky smart meter, and for the other half with another model of smart meters. These experiments also involve sociologists who will try to interpret the end-customers’ perception of their own metering data and energy consumption profile (and maybe how to raise their energy awareness).

The idea is to define the best strategies (the most convincing ones) for these customers to opt-in for self-effacing low-energy consumption behaviours at peak times (to reduce the stress on the grid), most probably through tariff incentives.

Some suggested programs could allow the utility provider to remotely turn-off a selected list of appliances or to lower thermostat settings during peak times. As well as providing personalized tips for better energy-efficiency, the end-user interface could encourage dwellers to participate in individual or collective challenges or to share their experience with their community and learn best practices on social networks.

It is expected that these guided interactions with their end-users would allow utility providers to improve their forecasting and profitability through advanced analytics and behavioural profiling.

factures its own energy gateways and smart metering plugs to monitor electrical appliances consumption and control them remotely. Other smartgrid-related devices include remotely controllable thermostats, temperature and hygrometry sensors or motion and open/close switch detectors that can send SMS alerts in case of intrusion suspicion.

Home Technology – www.home-technology.eu – was also exhibiting a so-called smart home gateway together with various sensors and actuators enabling dwellers to manage their home locally or remotely, either via a broadband connection or through the mobile GPRS network (thanks to an integrated SIM card).

On a larger scale, numerous smart grid projects are under way in the form of so-called eco-districts, specifically designed as experimental grounds to develop optimised energy-management solutions.

A 50/50 joint venture created in 2001 between Alstom and Bouygues, Embix provides energy-management services for such eco-districts, liaising directly with local authorities and building owners, managers or tenants to optimise smart grid resources at district level.

The company intervenes early in the district’s development phase and then pilots the energy optimization at the neighbourhood-level through its Urban Power platform, delivered via the cloud as SaaS (Software as a Service). The platform integrates all accessible real-time smart-metering data together with local energy production and storage fluxes.

One such project is IssyGrid in the Seine Ouest business district in Issy-les-Moulineaux near Paris. Jointly supported by Microsoft, Bouygues Immobilier, Bouygues Telecom, Schneider Electric, Total, Alstom, ERDF, ETDE and Steria, the project initiated in 2012 now covers the needs of nearly 10,000 people in a 160,000 square-meter area. It is expected to include nearby
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residential buildings in 2013.

At the European level, the Grid4EU large-scale demonstration project brings together a consortium of six European energy distributors (ERDF, Enel Distribuzione, Iberdrola, CEZ Distribuzione, Vattenfall Eldistribution and RWE) to test the potential of smart grids in areas such as renewable energy integration, electric vehicle development, grid automation, energy storage, energy efficiency and load reduction.

Six demonstrators will be tested over a period of four years (ending in 2016) in each of the European countries represented in the consortium. One of the demonstrators currently in progress is Nice Grid (in Carros, South of France), regrouping 1 500 end-customers. It explores renewable energy generation with 200 solar rooftops, integrates 100 batteries equivalent to 2MWh of storage capacity, and implements load curtailment with smart home equipment. Such large-scale projects help utility providers to test new forecast algorithms and figure out ways to reduce consumption levels during peak demand.

Founded in 2011 and spun-off from Minatec, Vesta-System markets its analytical software solution, VestaEnergy, to help office and residential building promoters anticipate future energy management needs. The dynamic software solution not only addresses the dynamics of real time energy metering and smart home connected sensors, it also brings into the equation weather conditions and predictions, energy price fluctuations and availability (distant, local and ultra-local sources in the case of connected buildings) to offer more accurate and individualized energy optimisation choices (not just routine energy profiles). The tool will be a central piece of the urban project Lyon Confluence 2 which will include 16000m² of private apartments and social housings. All the new occupants will be given access to their energy-consumption data through a digital tablet in order to better control their energy consumption according to their comfort zone (with the usual incentives for self-effacement).

**A dedicated communication network for the IoT**

Now to communicate their data, most of the smart meters and sensors spread out in these buildings could rely on ZigBee, an Ethernet connection to a local broadband access, sometimes a Power Line Communication link, a GSM module, an existing WiFi spot or some other proprietary RF link.

For low data throughput applications such as sensor messaging and remote smart metering, these technologies are overkill according to Ludovic Le Moan, CEO of Sigfox, a company that recently celebrated the first anniversary of what it claims to be the world’s first low-power cellular infrastructure dedicated to the Internet-of-Things. Sigfox’ technology builds upon ultra narrow band radio, combined with software defined radio techniques performed at base stations level to achieve a very high sensitivity for very long distance communications (from and 3 to 10km in urban areas, 30 to 50km in rural areas and over 1000km for outdoor objects sending messages in line of sight). The company offers its network services for as little as a dollar per year for the collection of IoT-emitted data (from any smart object equipped with the Sigfox radio) and for processing and routing it via the cloud to any third party application. One example the company gives is its partnership with MAAF Assurances, a leading French insurance company which will rely on the Sigfox network to offer fire and/or intrusion alert services to its customers directly through SMS. For now, Sigfox’ network covers France, but the company has big plans for expansion in Europe. By operating separately from traditional cellular networks, this IoT network infrastructure has the potential to save hundreds of megawatt/hour in a world with billions of connected objects, says the company.

Vesta System’s dynamic software solution for interconnected buildings provides accurate and individualized energy optimisation choices.

Sigfox’ low data throughput IoT network infrastructure could prove more economical than traditional carriers.
Multicore systems face the tools challenge

By Nick Flaherty

THE MOVE TO MORE HETEROGENEOUS multicore systems is going to fundamentally change the way code is developed in mobile, says a leading IP supplier. “This is the most exciting decade I have seen for computing,” said Tony King-Smith, executive vice president of marketing at Imagination Technologies, talking at the Multicore Challenge Conference run by verification expert Tvs. “There are opportunities to lead this global change here in the UK.

He points to the increasing split in the mobile market between ARM and other processor architectures all running different versions of Google’s open source Android operating system.

Intel has started to have some success with x86-based Atom processors in mobile handsets and tablets, while Imagination has acquired the MIPS processor line and is combining this with its PowerVR graphics and video technology and its programmable radio front end. Coupled with the move to technologies such as ray tracing, this creates a widely varying set of requirements, he says.

“We have three architectures in the Android world but the apps have to be able to traverse CPUs in the same way they do across GPUs and radios. We have to break this dependency on the CPU instruction set architecture and this is part of the future for heterogeneous processing,” said King-Smith. “Google is well aware of this problem,” he said.

There are different ways to tackle this issue, he says, including new capabilities in the LLVM tool chain (see box). “We are quite excited about LLVM and the portable binary format with binary translation,” he said. Another exciting approach actually changes the way systems are developed. Instead of downloading an app for a particular ISA, a generic app is downloaded that investigates what hardware resources are available. This ‘discovery’ app could be written with LLVM’s binary translation capability or a higher level language such as Java.

Once the discovery app determines the hardware available, it downloads different optimized blocks for the different hardware elements, creating the optimal software. This is not simple to do. “Discovery will be a fertile area for research and innovation,” said King-Smith.

More importantly it also changes the way the software is developed, he says. Instead of starting off with the data structures, you start with the discovery app. That provides the base software that is already available, and the developer then fills in the gaps in the software ecosystem, concentrating on the added value rather than re-inventing software for multiple different platforms.

Putting all this together with the right balance of memory and performance determines the power consumption and performance of the system. “This is a very key area,” he said. “Attention to detail makes a huge difference. I’ve seen four to five times the performance difference using exactly the same set of IP, so getting the balance is utterly key in making these systems work.”

The tool issue is the main reason why multicore computing has been slow to take off, says Prof David May at the University of Bristol. He points to homogeneous architectures where the programming is significantly easier. This was the approach he took with the multicore system used by XMOS Semiconductor where he is a founder.

Fig. 1: Imagination Technologies sees a discovery tool that looks at the hardware and downloads the relevant optimized code to build the code base for heterogeneous multicore devices.
He also points to older languages such as Fortran which include more support for parallel operation than modern day C and C++. However, there is a lot of focus on the parallel capabilities being added to these languages. Paul Keir of developer CodePlay in Edinburgh points to the C++ AMP 1.0 specification that is available for asymmetric multiprocessing, with a Microsoft implementation included with Visual Studio 2012. The CommitteeMP Draft (CD) of C++14 is out for Public Review, while OpenMP 4.0 is expected this summer with Release Candidate 2 now available for public comments.

The next OpenCL, OpenCL HLM, will include C/C++ syntax/compiler extensions, and there are even a new version of Fortran, Fortran 201x, in development. Combining the debugging and profiling tools pays dividends, says David Lecomber, COO of Warwick-based high performance computing tool vendor Allinea, who demonstrated the tools at the multicore Conference.

“Scientists, students, and developers learn once and win twice as they profile and debug their code with two tools that look and feel the same,” said Lecomber.

With the release of version 4.1, developers and scientists can use Allinea DDT and Allinea MAP interchangeably. “This joint licensing option is a natural progression that brings value to our customers. HPC centers are already telling us that adopting one part of the tool-suite encourages the adoption of the other amongst their users.”

“We’ve noticed fluidity in the workflow. A developer uses Allinea DDT to get the code right, then Allinea MAP to understand its performance, and then flicks back into Allinea DDT to uncover a performance issue’s root cause,” says Mark O’Connor, Allinea’s VP of Product Management. “We wanted to support that.”

Working between Allinea DDT and Allinea MAP is of particular interest to organizations like Cenaero, an applied research center in Belgium that develops simulation methods and software tools.

Last year, it was appointed by the Wallonian Minister of Research to operate a Tier-1 supercomputer, which will extend its current cluster of 3,000 cores to more than 10,000 cores.

One of the missing aspects of HPC storage is the analysis and understanding of the I/O patterns of applications. Allinea MAP now provides key metrics, such as the rates of read/write calls and uncached data transfer, making it easy to spot and diagnose lines of code with slow I/O performance in serial and parallel applications.

“But scientists and developers, who face a combination of software problems and pressure to advance their research, often opt for the false economy of trying things without taking the time to log them,” said O’Connor. Allinea DDT 4.1 automatically, records actions taken and the variables seen so developers can check the current code against the behavior of a previous version or even run it on a different system.

Allinea DDT 4.1 has also brought version control right into the code display, showing the age of different lines of code along with messages people wrote to describe their changes.

“When you’ve got this information, it’s much easier to fix the root cause of problems,” says O’Connor. “It’s a powerful debugging aid and there is nothing else like it on the HPC market.”

GCC vs LLVM: It’s all about the skills as $99 supercomputer ships

SOUTHAMPTON-BASED tool chain provider Embecosm has developed a full GNU Compiler Collection (GCC) tool chain for a new low power multicore processor that raised its development money on the Kickstarter startup web site.

US-based Adapteva raised nearly $1m from supporters on Kickstarter to develop a 2W, 64 core, 100GFLOP device on 28nm, and the $99 board started shipping in June. Embecosm has one of the early development boards for working on the tool chain. “It’s a 5 stage, dual issue pipeline and each processor has its own local memory and we un-roll the code loops to get the performance,” said Dr Jeremy Bennett, founder and CEO of Embecosm. “We have a version of GCC that gives pipeline occupancy of over 70%, and that comes from a deep knowledge of GCC with the loop unrolling. There are probably 50 good GCC engines in the world and we have one of them.” The demonstration shows a 512 matrix calculation handled in 68ms rather than seconds. “This is the level of performance we need for Software Defined Radio,” he said.

There are three other companies working on Low Level Virtual Machine (LLVM) for the Adapteva part. “What we see with LLVM is, as a compiler it is good, taking the 30 years of experience since GCC,” said Bennett. “What I see as a difficulty is the big players driving it, ARM, Qualcomm, Intel. There are 8 architectures in the standard distribution compared to over 40 in GCC.”

One reason for going to LLVM is the less restrictive license conditions. “The GPL license forces GCC to be kept together. LLVM makes it easier for people to do their own thing and not come together and that’s a weakness,” he said.

But that also means there are more engineers working with LLVM. “With LLVM a good software engineer can be up to speed in a year or so,” said Bennett. “Having them both means there’s rivalry and that incredibly healthy for the ecosystem.”
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Organic electronics another step closer to commercialisation

By Christoph Hammerschmidt

ORGANIC AND PRINTED electronics has been a promise for the future - over ten years or more. But now the technology is ready for commercialization, believes Wolfgang Mildner, president of industry association OE-A (Organic and Printed Electronics Association). At the LOPE-C organic electronics trade fair recently held in Munich, he claimed that this technology already became commonplace in a number of applications, in particular in automotive pharmaceuticals and packaging industries.

Mildner cited printed antennae and seat occupancy sensors which are said to be already in use in the automotive industry. The next steps will be the availability of touch sensors and displays for deployment in vehicles. At the fair, the OE-A also distributed a brochure with printed batteries and LEDs integrated into the front cover - upon the push of an equally printed button, the LEDs were lit – see figure 1. In order to drive commercial viability, "it now is necessary to refine the technology, but also to rethink it at some points where the dynamics of this technology and its markets have changed," Mildner said.

Towards this end, the industry association also introduced a modified roadmap for the further development of this technology and its commercialization. The roadmap breaks the technology down into five segments - organic photovoltaics, flexible displays, OLED lighting, electronics and components, and integrated smart systems – see figure 2. At the present level, the technology is at a stage where relatively simple products are possible - for example, portable chargers in the field of organic photovoltaics, or garments with integrated sensors, or anti-theft products in the segment of integrated smart systems. The state of OLED technology only permits design studies.

The roadmap now states the goals in the short, medium and long term. In the segment of organic photovoltaics, these goals include, for example, customized mobile power; in the segment of flexible displays, the companies organized in the OE-A intend to develop bendable OLED displays, plastic LCD, orrollable colour displays. In OLED lighting, they are going for transparent and decorative lighting modules. Short term refers to the time span from 2014 to 2016.

Long-term goals (year 2021 and beyond) include building integration and grid connection for the segment of organic photovoltaics,rollable OLED TVs and telemedicine applications in the segment of flexible displays, while OLED lighting will be part of the general lighting technology. In the field of electronics and components, the scientists regard directly printed batteries as long-term goals, and in the integrated smart systems segment, OLEDs will be integrated into garments, and health monitoring systems will be made of organic electronic parts - to name just a few goals.

During a presentation at the fair, Audi discussed its "Swarm" study of an OLED-lit car body – see figure 3. While the mock-up offers a spectacular look, the technology is not quite ready for real-world deployment, particularly not for automotive requirements. "OLED is the right technology, but it is not yet up to automotive standards", said Stephan Berlitz, Head of Lighting Innovations at Audi.

The main challenge remains the lifetime of the delicate electronics. The curved OLEDs don't withstand bad weather conditions, and also at very high or low temperatures they tend to fail. Another issue is cost, Berlitz admitted. Nevertheless, he insisted, OLED will have a great future. "The entire automotive industry has already begun to integrate OLEDs into their cars," he said.
Single die MEMS oscillator hits the mainstream

By Nick Flaherty

SILICON LABS HAS PORTED the low temperature MEMs technology it acquired with startup Silicon Clocks in 2010 to Chinese foundry SMIC. This allows a SiGe structure to be built on top of the passivation layer of a CMOS logic chip using the existing CMOS production line and eliminates the drift problems of dual die devices as the materials are specifically chosen to counteract thermal drift.

The programmable oscillators run up to 100MHz with frequency stability down to 20ppm and are aimed at cost-sensitive, low-power and high-volume industrial, embedded and consumer electronics applications such as digital cameras, storage and memory, ATM machines, point-of-sale equipment and multi-function printers. Higher speed devices are planned, says Mike Petrowski, vice president and general manager of Silicon Labs’ timing products.

The CMOS MEMs (CMEMS) technology enables guaranteed data sheet performance with 10 years of frequency stability including solder shift, load pulling, VDD variation, operating temperature range, vibration and shock. This guaranteed operating life performance is 10 times longer than typically offered by comparable crystal and MEMS oscillators. The oscillators tightly couple the MEMs resonator with CMOS temperature sensor and compensation circuitry, ensuring a highly stable frequency output in the face of thermal transients and over the full industrial temperature range. The end result is a predictable, reliable frequency reference over the long operating lifespans of industrial and embedded applications.

The Si50x CMEMS oscillators support any frequency between 32 kHz and 100 MHz. Frequency stability options include ±20, ±30 and ±50 ppm across extended commercial (-20 to 70°C) and industrial (-40 to 85°C) operating temperature ranges. The CMEMS oscillators also offer extensive field- and factory-programmable features including low-power and low-period jitter modes, programmable rise/fall times and polarity-configurable output-enable functionality.

Using CMOS MEMs rather than a crystal frees customers from supply chain problems that are typical for traditional quartz-based solutions. Because CMEMS oscillators are integrated, monolithic ICs, they are packaged in widely produced, molded-compound 4-pin packages, again ensuring a predictable and reliable supply chain.

Printing microbatteries could unravel new designs in medical applications

By Julien Happich

A TEAM BASED AT HARVARD UNIVERSITY and the University of Illinois at Urbana-Champaign, has demonstrated how 3D printing can now be used to print lithium-ion microbatteries the size of a grain of sand, which could be small enough to fit in tiny devices for medical or communications applications.

In recent years engineers have invented many miniaturized devices, including medical implants, flying insect-like robots, and tiny cameras and microphones that fit on a pair of glasses. But often the batteries that power them are as large or larger than the devices themselves, which defeats the purpose of building small. To get around this problem, manufacturers have traditionally deposited thin films of solid materials to build the electrodes. However, due to their ultra-thin design, these solid-state micro-batteries do not pack sufficient energy to power tomorrow’s miniaturized devices.

The scientists realized they could pack more energy if they could create stacks of tightly interlaced, ultrathin electrodes that were built out of plane. For this they turned to 3D printing. 3D printers follow instructions from three-dimensional computer drawings, depositing successive layers of material—inks—to build a physical object from the ground up, much like stacking a deck of cards one at a time. The researchers have designed a broad range of functional inks—inks with useful chemical and electrical properties. And they have used those inks with their custom-built 3D printers to create precise structures with the electronic, optical, mechanical, or biologically relevant properties they want.

The researchers created an ink for the anode with nanoparticles of one lithium metal oxide compound, and an ink for the cathode from nanoparticles of another. The printer deposited the inks onto the teeth of two gold combs, creating a tightly interlaced stack of anodes and cathodes.

The electrodes were then packaged into a tiny container filled with an electrolyte solution. The electrochemical performance is claimed to be comparable to commercial batteries in terms of charge and discharge rate, cycle life and energy densities.
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Watch the video
**Direct semiconductor wafer bonds target next-gen solar cells**

By Julien Happich

**THE FRAUNHOFER INSTITUTE FOR SOLAR ENERGY SYSTEMS** (Fraunhofer ISE) today has joined forces with EV Group (EUVG) to develop equipment and process technology to enable electrically conductive and optically transparent direct wafer bonds at room temperature. The new solutions, developed in partnership with Fraunhofer ISE based on EVG’s recently announced ComBond technology aim to enable highly mismatched material combinations like gallium arsenide (GaAs) on silicon, GaAs on indium phosphide (InP), InP on germanium (Ge) and GaAs on gallium antimonide (GaSb).

Direct wafer bonding provides the ability to combine a variety of materials with optimal properties for integration into multi-junction solar cells, which can lead to new device architectures with unparalleled performance.

“Using direct semiconductor bond technology developed in cooperation with EVG, we expect that the best material choices for multi-junction solar cell devices will become available and allow us to increase the conversion efficiency toward 50 percent,” stated Dr. Frank Dimroth, Head of department III-V – Epitaxy and Solar Cells of Fraunhofer ISE.

“We are excited to partner with EVG, a leading supplier of wafer bonding equipment, to develop industrial tools and processes for this application.” Fraunhofer ISE has developed III-V multi-junction solar cells for more than 20 years and has reached record device efficiencies of up to 41 percent with its metamorphic triple-junction solar cell technology on Ge. Higher efficiencies require the development of four- and five-junction solar cells with new material combinations to span the full absorption range of the sun’s spectrum between 300-2000 nm. Integration of III-V solar cells on silicon opens another opportunity to reduce manufacturing cost, especially when combined with modern substrate lift-off technologies. Direct wafer-bonding is expected to play an important role in the development of next-generation III-V solar cell devices with applications in space as well as in terrestrial concentrator photovoltaics (CPV).

EUVG’s ComBond technology has been developed in response to market needs for more sophisticated integration processes for combining materials with different lattice constant and coefficient of thermal expansion (CTE). The process and equipment technology enables the formation of bond interfaces between heterogeneous materials—such as silicon to compound semiconductors, compound semiconductors to compound semiconductors, Ge to silicon and Ge to compound semiconductors—at room temperature, while achieving excellent bonding strength.

The ComBond technology will be commercially available later this year on a new 200-mm modular platform currently in development, called EVG880 ComBond, which will include process modules that are designed to perform surface preparation processes on both semiconductor materials and metals.
Toyota connects navigation systems to the cloud

By Christoph Hammerschmidt

A NEW TRAFFIC INFORMATION system for Toyota drivers blends a variety of parameters including vehicle location data, current speed, road conditions and even disasters. The concurrent utilization of these data helps optimizing routes and travel times.

The “Big Data Traffic Information Service” gathers traffic flow data from several telematics services. These swarm data are collected, stored and enriched by contributed data from specific commercial user groups such as emergency services or forward agencies. From all these data a live traffic flow map is generated and made accessible to users. The purpose of the service is to improve overall traffic flow and enable trade-specific navigation services. In addition, the service is designed to enable faster emergency services in the case of catastrophic events such as earthquakes. Besides Toyota drivers, also subscribers of Toyota’s G-BOOK telematics service for smartphones can access these data and use them to optimize their travel route.

This cloud-based service allows the use of traffic information gathered by Toyota and provides information on routes and traffic density on specific trajectories. All data are fed into the in-car navigation systems, but they also can be accessed through computers, tablets or smartphones. The service displays a great variety of additional information from the authorities; it also displays the location of emergency services and vehicles. Users can add their own data.

Information about facilities owned or operated by local governments and businesses and locations of commercial vehicles can be shown on the map, while information and images can be submitted by users via smartphones.

In disaster situations, information about evacuation sites, shelters, and other facilities can be shown, with the location of rescuers (equipped with smartphones) and emergency and relief vehicles also indicated on the map.

To facilitate damage assessment and relief efforts during times of emergency, rescue personnel can submit damage information and make relief requests via smartphone, with this information being shown along with T-Probe traffic information, route history, and hazard maps provided by local governments.

At other times, the service can be used for traffic and logistics systems. Suitable processing of T-Probe traffic information enables map-based route planning for effective guidance to multiple destinations, along with location tracking and travel history management.

The service will be available initially in Japan, Toyota said.

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Intel joins A4WP wireless charging group

By Peter Clarke

INTEL HAS JOINED THE ALLIANCE for Wireless Power (A4WP) consortium and taken a seat on the board of directors along with Broadcom, Gill Industries, IDT, Qualcomm, Samsung Electronics and Samsung Electro-Mechanics.

The move will put weight behind A4WP which is a rival standards organization to the Wireless Power Consortium (WPC), seeking to provide wireless charging for portable consumer electronics devices, including, smartphones, tablet, netbook and laptop computers.

WPC was the first to market and claims as many as 8.5 million products have shipped using its Qi technology, some based on chips announced last fall by Texas Instruments. Intel demonstrated its own technology.

A4WP, which specifies the use of magnetic resonance technology, is capable of simultaneous charging of multiples devices and the flexible positioning of devices and a charging platter.

“Intel believes the A4WP specification, particularly the use of near field magnetic resonance technology, can provide a compelling consumer experience and enable new usage models that make device charging almost automatic,” said Navin Shenoy, general manager of the mobile client platform division at Intel, in a statement issued by A4WP.

The A4WP mission includes development of industry specifications for submission to national and international standards development organizations, management of an A4WP certification program, including consumer-recognizable certification logo and the coordination with national and international regulatory agencies regarding policy and compliance.
Non-volatile CBRAM memory block operates at less than 1V

By Julien Happich

ADESTO TECHNOLOGIES HAS presented a paper on the ultra-low power operation of its proprietary CBRAM (Conductive Bridging RAM) memory at the 2013 Symposium on VLSI Technology and Circuits in Kyoto, Japan. The paper explores the use of the non-volatile memory technology embedded in a body sensor, a device developed to operate without a battery in the system, through the use of energy harvesting.

The paper follows the successful completion of a project in cooperation with a team of technologists from the University of Virginia to create a low energy device to acquire physiological data from the human body, process that data, and transfer it through wireless communication. The project was partially funded by DARPA through the US government's program to invest in and award small business innovation research (SBIR).

CBRAM is an emerging, disruptive memory technology which can be integrated in standard CMOS processes, function as a discrete memory device or be embedded in microcontrollers, System-on-Chip (SOC) or Field Programmable Gate Arrays (FPGA). The paper demonstrates the ability of a non-volatile CBRAM memory block to operate at less than 1V supply voltage for read, program and erase functions without the need for charge pumps. This low-power functionality translates to 3x lower write voltage and approximately 10x lower write energy compared to other low energy non-volatile memory devices.

“We have built some exciting wearable wireless body sensors that run completely without batteries from body heat, but one key missing piece was non-volatile memory (NVM). Existing NVM devices are way too power-hungry for our aggressive power budgets,” said Ben Calhoun, associate professor at the University of Virginia. “This integrated ultra-low-power CBRAM from Adesto is an important advance for self-powered systems.”

“Ultra-low energy non-volatile memory like CBRAM is essential to the development of energy starved technologies that require stored instructions and data collection over an extended period,” said Shane Hollmer, VP of Engineering at Adesto. “These devices must preserve data even in the event of power interruptions and failures. CBRAM is a natural fit for these applications.”
Version control in EDA for optimum hardware design

By Robert Huxel

AS A TYPICAL PRACTICE, most large EDA vendors conduct a costly on-site case study of a prospective client’s existing system at a cost that can run into the millions of dollars. In the next step of the scenario, they deploy a Field Application Engineer (FAE) on site to manually produce code. The objective: an integrated design solution. Instead, the result produces a lengthy and costly process that often fails to integrate even a majority of the prospect’s desired functionality, especially for version control.

Unfortunately, electronic engineering educators typically do not teach version control. Version control actually evolved as a software best practice methodology. It became an absolute necessity for software developers because programs grew to such large sizes that they required ever larger design teams. Trying to manage the volumes of code without an effective version control system provides an excellent definition of hell. Version control allows multiple team members to be simultaneously working on a software program without risk of losing or overwriting another member’s code.

Complexity in software development

Over the past 20 years, software programs have grown rapidly and become more complex. With each new software release, the code needed to be regularly updated to incorporate new or improved features and bug fixes. To cope, the software industry implemented modular design practices, a form of design reuse.

Companies found that reusing software modules delivered many benefits. Modules resulted in increased dependability because reused software has already been tested in working systems. Reuse also reduced process risk, since the functionality, risk, and cost of existing software was already known. In addition, reusable software makes effective use of specialists, since the software embodies their knowledge. Perhaps most compelling, design teams realized that reuse resulted in accelerated development, reducing the time spent in coding and validation. As a result, they could meet accelerated time-to-market objectives and produce new iterations of product versions faster.

However, implementing software design reuse did not come without its challenges. Generalized application of software modules doesn’t just happen. First, the modules must be maintained and development processes adapted in subsequent releases. Reused modules may also become increasingly incompatible with system changes in subsequent releases, resulting in increased maintenance costs. To actually have value, reused elements must be discoverable in the library, understood, and sometimes adapted. In subsequent versions, new or upgraded design elements will likely impose prerequisites and dependencies to which the reused elements must comply. Perhaps most challenging in the IP ecosystem, many companies believe they can and should rewrite components because they believe they can improve or own them.

Software complexity leads to team approach

In a development team environment, multiple people touch the same code. To manage the team, engineering managers need visibility of their team’s work. As a first requirement, the team needed a single secure storage repository for their various design modules. Once established, the design team needed an incremental history of changes made to the source code. To achieve effective reuse in a team environment therefore also required an effective method to check-in and check-out design sources.

Fig. 1: Aberdeen Group’s research report, “Need to Save PCB Design Time?” established three categories of survey participants: best-in-class, average, and laggards.

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changes made to the source code in real-time. This also meant that the system captured metadata for each change, including who made the change. This facilitated full traceability, meaning the ability to document which team member worked on which module, made what changes, and when. It also enabled improved reporting and monitoring so engineering managers could track productivity and design progress. All of these advances resulted in accountability by all team members.

**Version control for hardware design**

PCB design teams can typically range from one to 20 designers with an average of approximately five for mainstream design firms. Large semiconductor companies may employ FAE teams numbering in the hundreds who do reference design work. Commonly, small to medium hardware design teams maintain electronics design data on each designer’s individual hard drives. Unfortunately, no one then actually knows where all the data for the design is located.

As companies have realized this shortcoming, they have committed to maintaining their corporate knowledge in a dedicated database. Electronics hardware design teams have had some difficulty implementing version control because the process and tools are still largely based on software engineering principles. Without an integrated version control system in their EDA tools, hardware designers have tried freestanding version control programs with check-in and check-out capabilities. However, non-integrated solutions fall down because the individual designer and/or the manager can make no visual comparisons to the schematic and the PCB from one version to the next.

In EDA software with fully integrated version control, team members see the status of all templates, updates to relevant regulatory standards, and changes to any designs. As a result all team members are automatically notified when a change occurs. In software, a manager or team member can run a “differencing tool” in the software under development to identify, resolve and commit changes between versions.

However, EDA tools produce binary and graphical output, not text based output as in software code. This makes identifying hardware changes via a text-based, non-integrated tool extremely difficult and error-prone. Managers and designers need to see the changes graphically, merge them into the design, and commit to the change. Simply put, none of these capabilities are possible with non-integrated version control systems.

**Adjusting hardware design best practices**

Hardware design practices need to change due to competitive pressures as noted in the Aberdeen Group’s research report, “Need to Save PCB Design Time?” The report is based on interviews and surveys of 133 electronics companies. Once the research team gathered all of the data, they assembled a competitive assessment of the surveyed companies. They established three categories of survey participants: best-in-class, average, and laggards.

As shown in the survey, each of the three categories of companies exhibited common performance levels for five key parameters:

- **Process** (the approaches they take to manage PCB data)
- **Organization** (who data is exposed to)
- **Knowledge Management** (how the knowledge in the PCB data is managed)
- **Performance Management** (the ability of the organization to measure its results to improve its PCB data management practices)
- **Technology** (the appropriate tools used to support PCB data management)

Version control, as noted in the Aberdeen report, falls into the category of “Knowledge Management”. Note that the “Knowledge” category in figure 1 cites three items:

- Schematics and PCB layout are synchronized
- Schematics and BOM are synchronized
- And there is version control for each data element on the PCB

Any stand-alone version control software can perform basic check-in and check-out. However, design teams quickly discover that they can’t automatically lock a checked-out item. This results in either overwritten or lost design work. Team participants are also unable to visually compare revisions in the schematic or the PCB. They also painfully learn that the solution lacks built-in data management functionality. Merging collaborative work performed on different parts of the project poses further time-consuming challenges.

EDA tools with an integrated version control system (VCS) deliver full check-in and check-out functionality including locking of checked-out items. Like their software counterparts, an integrated VCS establishes a single repository for all projects. All design modules and components are checked into the Version Control Repository.

Each individual file contains extensive meta-data including a record of design changes, the designer, date of change, etc see figure 2.

When two (or more) team members simultaneously check out an item, the file is formally checked out to the first user. Depending on the actual version control backend, the user either automatically or manually locks the file from any other team members. When a second user checks out the same file, this designer can work on it only as a copy. Once the first designer completes work on the file and saves it to the repository, that action releases the lock. When the second designer reopens the now unlocked file, his work will be marked “out of date”. He or she can review the changes made by the first designer and merge the work previously done as a copy into the file and check it back in if appropriate.

To establish an incremental history, the project’s engineering manager performs the initial check-in and labels the project as REV 0. This becomes the starting point for the design.
Ultra high definition broadcast equipment, 400G Ethernet systems and computer data centres – all feast on vast quantities of data. Consuming and processing that level of data with any electronic system is difficult. You will need to be at the leading edge of technology, both with the architecture you use to process the data and the manufacturing process you use to generate the device.

FPGAs have for many years been at the forefront of technology, Moore’s law has been kind to FPGAs - with the right process/architecture design decisions you can reduce power, increase performance and reduce cost/increase density at each generation. Each generation of FPGA captures more applications that previously would have had to be designed with ASICs, and opens a new market due to the performance, flexibility, power or cost that couldn’t be reached with the older technology.

There are three key aspects to consider when creating an ideal modern FPGA.

- Leading-edge manufacturing processes technology
- Investments in innovative architecture and IP
- High-performance integration of processors with programmable fabric

Most process-technology foundry suppliers are in the early test chip stages of FinFET. At the time of writing, Intel is the only manufacturer who has production quality products shipping using a 3D (Tri-gate) transistor technology. Customers looking and asking for performance improvements will not get this from 3D transistor technology alone, but they will also need a process shrink. The recently announced 14 nm Tri-Gate process from Intel provides this process technology. Altera’s future Stratix 10 FPGAs will be built using Intel’s 14 nm Tri-Gate process.

Process is only part of the story; Altera is currently developing a new architecture which is capable of astonishing core speeds of up to 1 GHz. The enhancements to the digital signal processing (DSP) architecture deliver a dramatic improvement to DSP capability enabling over 10 TLOPs of single precision floating point operations. Transceiver performance also gets a boost with the ability to run at up to 56 Gbps data rates.

Within the Generation 10 portfolio Arria 10 FPGAs use a 20 nm planar transistor process to implement sixteen 28 Gbps transceivers for next-generation multi-100G optical interfaces. With enhanced signal conditioning techniques, such as adaptive decision feedback equalizers (DFE), and hardened forward error correction (FEC), high loss backplane applications can be addressed.

**Processor Integration**

FPGA integration of discrete components on a board has reduced the complexity and cost of many customer systems, but one of the most important changes has been the recent integration of an ARM-based hard processor sub-system (HPS). Altera Arria 10 SoCs offer enhanced dual core ARM Cortex™-A9 HPS, this is a boost for customers wanting tighter integration between CPU and FPGA fabric. The next generation HPS is shown in Figure 3.

Figure 1: Tri-Gate Process Technology

Figure 2: 28 Gbps Operation on 20 nm Process Technology from Altera

Figure 3: Second-Generation HPS Block with ARM Cortex-A9 Processor

Next-Generation FPGAs and SoCs Are Coming

Altera uses a tailored innovative approach to portfolio design, coupling new architectures to the latest process technology to bring together an exciting suite of FPGAs. It’s fair to say the Generation 10 portfolio will have the largest leap in capabilities that hardware architects and system designers are yet to see thus far in an FPGA.
All changes are subsequently only maintained incrementally. Since repeatedly saving the complete design as a new revision number takes up enormous volumes of data storage space, the system only saves the incremental changes.

One potential source of design changes is a process referred to as “branching”. Branching allows the design team to explore “what-if” scenarios as a branch of the main line of development. Any authorized team member can establish a branch at any point in the main development line. If V1.0 is released, branching allows for minor fixes. Branching allows for these fixes, if appropriate, to be incorporated into subsequent product releases. Design teams using EDA tools with a fully integrated version control system experience many benefits, the first of which is a reduction in errors.

Accountability and productivity improve because each engineer can view who is making changes in the design and see that engineer’s work. Each team member can then readily ask questions of that designer regarding that specific change. Further, because all team members can see each other’s work, productivity improves.

After implementing an integrated VCS, documentation and reporting also improve. Each time a team member checks a file back in, he or she must add a comment. This facilitates project management, QA, and standards compliance to get products certified to current relevant industry standards. Further, with full graphic and onscreen visual comparisons between two different revisions, team members can view highlighted changes side-by-side.

Altium Designer answers the version control needs of hardware design teams. It delivers the only fully integrated EDA version control system. All design data are maintained in a single repository and the data remain fully synchronized. The system displays changes in up to four panels on screen. This advanced capability further highlights all changes in both the schematic and the PCB – see figure 3. All changes are also documented as text to enhance management oversight.

Timing closure highlights the challenges of 45nm silicon design and below

By Chi-Ping Hsu

INNOVATION IS THE CORNERSTONE of the semiconductor industry and has been responsible for massive changes in all parts of the industry, from design through fabrication, assembly and test. The foundational requirements of innovation in design are changing; they are expanding in scope. Point solutions that locally optimize a single design process by some metric, such as power, are more often than not proving to be a net disruption to design closure, rather than a benefit.

The necessarily expanded scope of innovation, especially true for advanced node design, means that the most significant innovations will come from large organizations that are willing to make bold investments.

We estimate that the EDA investment for the move to 20nm and 14nm FinFET to be in the $1B range. For the size of our industry, this is indeed a bold, albeit necessary, investment.

We can regard the issue of timing signoff as a microcosm of the way in which innovation in EDA has changed and how it is evolving now and into the future.

Cadence Design Systems has responded with the recent introduction of its Tempus Timing Signoff Solution, a new static and timing analysis closure tool that yields up to an order of magnitude faster than traditional timing analysis solutions.

Although start-ups have developed new technologies that solve individual parts of the signoff problem, those innovations sometimes do not make it through to the implementation flows used by system-on-chip (SoC) engineering teams because they do not solve the overarching problems.

Over the past decade and a half, the physics of nanometer technology have taken an increasingly firm grasp on the design process and created a much more complex situation for signoff. The shift from ASIC to SoC design that began in earnest at the start of this millennium accompanied a dramatic change in methodology and also the way in which innovative design technologies came to the market.

Just 15 years ago, signoff for digital logic-dominated designs was relatively straightforward thanks to the use of widely accepted approximations. Gate delay strongly outweighed wire delay, which could be treated as practically negligible. Signoff was largely a matter of performing timing analysis based on the results provided by the ASIC vendor’s ‘golden’ gate-level simulator.
Design teams gradually took on more of the responsibilities of signoff work from the ASIC vendors as they moved production to foundries. At the same time, layout-dependent effects played an increasing role in the performance of design. Gate delay moved to become less important on critical paths. Wire delay took over as the key issue to solve. This called for a new generation of layout-aware tools developed by both large, broad-based EDA tools suppliers and start-ups.

Start-ups played a crucial role with their technology. Each could tackle a hole in the offerings of mainstream suppliers by, very often, recruiting a small and select group of ‘teaching customers’ who could feed back vital information on tool performance from real designs. Engineers from these start-ups would often engage in close collaboration with the design teams inside the customers responsible for benchmarking and working with their software.

In recent years, many of the nanometer effects with which SoC design teams must engage have become closely interconnected. Just ten years ago, a timing violation on a critical path could easily have been solved by the insertion of a buffer, or the movement of some of the gates to reduce the wire distance and with it delay. A point tool optimized for this analysis and solution could easily be inserted into a broader design flow.

Analysis was often optimized for capacity rather than accuracy. As designs moved to millions of gates, runtime overhead was often the primary issue. Parasitics could, to a large extent, be abstracted out except for paths that were extremely close to the timing margin. At 130nm, for example, the gap between metal interconnect lines were such that their coupling capaci-
tances were overshadowed by ground and pin capacitance. For the inter-track coupling capacitance, it was generally easier and faster to add a small margin.

The number of timing runs was also quite limited. In general, it was sufficient to analyze a best-case, nominal and worst-case scenario for three of the key parameters: process, voltage and temperature. This would effectively encompass all the realistic operating points for the design on its target process. It was reasonable to make the assumption that delay would be at maximum temperature, lowest voltage and worst process conditions.

As process dimensions shrank, assumptions that previously held up well began to break down. The coupling capacitance between metal interconnect became much more significant at 65nm because the line pitch was much tighter and the traces themselves became taller in order to keep parasitic resistance under control. As a result, the lines began to behave more like the parallel plates of a capacitor.

At 45nm, the variation in metal thickness became a key concern, increasing the range over which designs needed to be simulated to provide best-case and worst-case delay values. Below 45nm, lithographically-induced variations in transistor, gate and local interconnect structures became significant, leading to the introduction of larger margins to accommodate the difference across the process variability range.

Other, more subtle, effects of the shift to nanometer dimensions have led to an explosion in the effort needed to achieve timing signoff.

The overarching issue is the interaction between global and local effects. Since the beginning of the past decade, behavior under temperature changes became more difficult to predict, a situation that has been given the name “temperature inversion dependence”. The issue is caused by the use of lower supply voltages in order to provide greater energy efficiency – see figure 1.

Instead of running faster than a ‘hot’ corner, the circuitry may run more slowly under a certain threshold voltage as the temperature falls – and the effect is dependent on the threshold voltage used in the devices that lie along the path being analyzed. The reason for the effect is that two effects combine to determine the delay through a logic gate. At the higher volt-
age used traditionally, mobility controls the drain current of an active transistor. But as voltages drop, the threshold voltage has a much larger role in determining drain current. As a result, old assumptions break down and demand that a larger number of analyses are needed to check properly for variations.

In nanometer processes, variability is more localized than it was on older processes. Metal line widths have become small enough to impact the resistance of the wire with just a small amount of variation. Given that metallization is a separate process from base layer processing, engineers cannot assume that process variations will move in the same direction for both base and metal layers. Therefore, at 45nm and to a larger extent at 28nm, multiple extraction corners were required for timing analysis and optimization.

Double patterning provides further source of variability in sub-28nm processes. Because lithography under double patterning calls for two masks for the same layer, the masks must be precisely aligned such that the spacing between patterns is consistent across the die. Although foundries are working hard to minimize the effect, there will always be some phase shift in the masks relative to each other and it may not be possible to predict what that phase shift is – see figure 2. Timing views are required that reflect the impact of phase shifts in different direc-
The problem is not just confined to the leading-edge processes. Increasingly, low-power design techniques are being applied to designs aimed at older processes. Although these processes will have fewer sources of variability, as voltages are reduced to take advantage of power savings, effects such as temperature dependence inversion become more apparent.

The time it takes to generate each timing view is only a small part of the problem. Up to 40 per cent of the chip implementation flow is now consumed by the time it takes to act on the results of the analyses – see figure 4. Each timing view generates a set of violations that need to be correlated with the results from the other timing views. Consolidating the data takes time, engineering insight and, for many teams today, custom scripts to process the data. There is then the issue of implementing the changes needed to close timing.

Today’s signoff timers are not physically aware. Any changes, such as buffer insertion, are left to the implementation environment as a post-processing step for engineering change order (ECO) generation. Often the placement of new cells is dramatically different from what is assumed by the optimization algorithms because available vacant space is hard to find in highly utilized designs.

The result is a significant mismatch between the assumed interconnect parasitics during the optimization steps and the actual placement and routing that result from the ECO. Changes may affect the timing of paths that may have already met timing, causing them to violate timing in the timing views from the subsequent iteration. What previously may have been a timing-clean view could potentially have many violations after placement and rerouting.

One thing becomes clear from an analysis of the way in which timing signoff has evolved over the past decade. A simple technology update is not enough to solve the problems. Conventional wisdom holds that startups provide much of the innovation for technologically driven markets. Startups have traditionally used ‘teaching customers’ to help drive them towards market-ready solutions. However, such solutions do not always make it to market because the need is no longer for narrowly defined solutions but for a tool infrastructure that cuts across the different pieces of the implementation flow.

A more accurate implementation engine would reduce some of the overhead of dealing with multiple timing views. But a genuine solution requires attention to multiple points in that flow, involving a more holistic approach.

There are numerous actors in the SoC ecosystem who can and do provide essential knowledge and feedback on issues that affect design and implementation. It is extremely difficult for a start-up with a more restricted set of partners to engage with all of them in order to derive the best solution. Although the core technology being delivered may have many strong points and provide better support for certain issues, the key today is to be able to bring all of the technology to build a more cohesive solution. It involves input from foundries and IDMs, with their knowledge of the way that variability issues affect timing. Library vendors have their part to play in understanding the issues caused by moves to smaller geometries and the impact of technologies such as double patterning. And there are the early adopter customers who can provide real-world designs that exercise all parts of a design flow.

Then there is the role of the EDA tools supplier to bring the inputs together and develop new ways of dealing with the influx of data. The supplier needs to have the scope to look at the flow in a holistic manner and understand which are the choke-points that limit design speed. A more accurate implementation engine for ECOS is one possible answer to the problem of timing signoff. But a more effective approach may be to look at the overarching requirements of signoff and to work out ways in which the application of timing fixes and ECOS are made so that they are more closely integrated with the timing signoff process. That requires a combination of new technology and attention to detail in the architecture of the overall flow that a player with decades of experience in implementation can bring.

As a result, the industry is moving towards a new development pipeline that involves a matrix of partnerships rather than individual links between design and tools-development groups. By bringing these different views together, EDA tools developers can react much more quickly to the needs of design and reflect the pace of innovation that is taking place in product design and process engineering.
Modeling skew requirements for interfacing protocol signals in an SoC

By Hans Kumar Jain, Gourav Kapoor and Babul Anunay

A SYSTEM ON A CHIP (SoC) today consists of several different microprocessor subsystems, memories and support for I/O interfaces such as JTAG, Ethernet, DSPI, SENT etc for communication with the outside world – see figure 1. All these are universally accepted and have some timing requirements which may be in form of input/output delay requirements or special timing requirements (like transition and skew requirements for different signals), which need to be taken care of at the STA end. In this article, we will be focusing on one of these – maximum and minimum skew between two signals.

Some of these protocols (like DDR) have requirement for a finite maximum skew (difference in delays) between the various signals of a bus. All data has to change within a very small timing window. On the contrary, minimum skew requirement is generally specified to prevent the race condition between two signals. This is usually one sided; e.g. signal ‘a’ should follow ‘b’ after some finite time. Until recently, these skew requirements were modeled in a roundabout manner and had to be updated regularly which adversely impacted the STA analysis time of each database as there were multiple iterations for IO constraints maturity. Also, the constrained signals’ timing may get deteriorated during optimization in the absence of constraints on these signals. There can be different ways of implementing this using multiple command combinations. Each has its own merits and demerits. Let’s look at three methods to achieve this purpose:

Applying minimum/maximum delay constraints

We can apply min and max delay constraints on data signals so that data changes only within a given window. This method can be used to constrain multiple signals for skew requirement as discussed below. We are essentially assuming these signals to change within a timing window and assuming the buffer to be large enough to overwhelm the timing window. This is a valid approach as the STA tool looks at the worst case scenario. You can also use this method to constrain the signals in read and write cycle, i.e. the timing pertains only to the write cycle in the read cycle.

Applying input/output delays

This method involves applying delay constraints on the output side to ensure that the signals meet the specified skew requirements. This can be useful if the signals are constrained at the input side with minimum/maximum delay constraints.

Applying setup/hold checks considering one of the data signals as reference signal

This method involves applying setup/hold checks on the data signals considering one of the signals as the reference signal. This can be useful in scenarios where the signals are constrained at the input side with minimum/maximum delay constraints.

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EDA & DESIGN TOOLS

have some characteristic delay range, which is a pure assumption or based on prior experience. The EDA command to apply min/max delay is:

\[
\text{set_min_delay/set_max_delay} \quad <\text{delay_value}> \quad \text{signal}
\]

A data bus can be constrained to be within a specific window by constraining each bit signal with min and max delays (where \(\text{max}_{-}\text{delay} > \text{min}_{-}\text{delay}\)) – see figure 2.

\[
\begin{align*}
\text{set_min_delay} & \quad <\text{min}_{-}\text{delay_value}> \quad \text{data\_bus}[*] \\
\text{set_max_delay} & \quad <\text{max}_{-}\text{delay_value}> \quad \text{data\_bus}[*]
\end{align*}
\]

The maximum skew requirement window will then be:

\[
\text{Max}_{-}\text{skew}_{-}\text{requirement} = \text{Max}_{-}\text{delay}_{-}\text{value} - \text{Min}_{-}\text{delay}_{-}\text{value}
\]

Similarly, the timing requirement for minimum skew can be justified by applying max_delay constraint to one signal (the one which is to occur first) and min_delay constraint to the other (the one which is to occur later – see figure 3).

\[
\begin{align*}
\text{set_max_delay} & \quad <\text{smaller}_{-}\text{value}> \quad \text{signal\_1} \\
\text{set_min_delay} & \quad <\text{larger}_{-}\text{value}> \quad \text{signal\_2}
\end{align*}
\]

Where:

\[
\text{Min}_{-}\text{skew}_{-}\text{requirement} = \text{Min}_{-}\text{delay}_{-}\text{value} - \text{Max}_{-}\text{delay}_{-}\text{value}
\]

The application of min/max delays offers some advantages, the uncertainty values applied on path don’t need to be taken into account and delays can be modified in any of the data signal path as long as the above conditions are met. This method, however, faces some limitations as it takes a couple of iterations to decide upon the values of the min-max delay.

\[
\begin{align*}
\text{Fig. 2: Constraining signals to be within window by applying min/max delays.}
\end{align*}
\]

Constraining IOs by modeling input/output delays

In this method, we define the relationship of interface signals with respect to some clock. We may use it to implicitly define skew requirement by defining input/output delays of different signals with respect to same clock such that they are constrained to have the required skew. Basically, by defining input and output delays, we are defining setup and hold timings of the signals in the SoC as seen from the outer world. The designer just needs to constrain these by defining valid and invalid windows. I/Os may be constrained in EDA tools using the following commands:

\[
\begin{align*}
\text{set_input_delay/set_output_delay} \quad <\text{delay}_{-}\text{value}> \quad \text{port\_name} -\text{min}/\text{-max}
\end{align*}
\]

To constrain signals to be within a timing window (maximum skew requirement) using this technique, we need to define setup and hold checks (min and max input delays) for all signals with respect to the same clock such that all signals are allowed to change nowhere except the required window - as shown in figure 4.

Considering both signals to be input signals,

\[
\begin{align*}
\text{max}_{-}\text{input}_{-}\text{delay} = \text{clock}_{-}\text{period} - \text{setup}_{-}\text{requirement} \\
\text{min}_{-}\text{input}_{-}\text{delay} = \text{hold}_{-}\text{requirement}
\end{align*}
\]

Under the condition

\[
\begin{align*}
\text{setup}_{-}\text{check}_{-}\text{for}_{-}\text{signal1} + \text{hold}_{-}\text{check}_{-}\text{for}_{-}\text{signal2} < \text{clock}_{-}\text{period} & \\
\text{setup}_{-}\text{check}_{-}\text{for}_{-}\text{signal2} + \text{hold}_{-}\text{check}_{-}\text{for}_{-}\text{signal1} < \text{clock}_{-}\text{period}
\end{align*}
\]

Similarly, we can constrain the signals for minimum skew requirement. For this, following condition should be kept in mind (for signal1 to follow signal2 – see figure 5):

\[
\begin{align*}
\text{Setup}_{-}\text{check}_{-}\text{for}_{-}\text{signal1} + \text{hold}_{-}\text{check}_{-}\text{for}_{-}\text{signal2} > \text{clock}_{-}\text{period}
\end{align*}
\]

\[
\begin{align*}
\text{Fig. 3: Constraining signals for minimum skew by applying min/max delay constraints.}
\end{align*}
\]

\[
\begin{align*}
\text{Fig. 4: Constraining signals to be within window by applying input/output delays.}
\end{align*}
\]
We can, thus, write as shown below:

\[
\begin{align*}
\text{set_input_delay} & \ <\text{max_input_delay}> \ \text{signal2} \ -\text{max} \\
\text{set_input_delay} & \ <\text{min_input_delay}> \ \text{signal1} \ -\text{min}
\end{align*}
\]

In a similar way, we can constrain the output signals too for skew requirement by applying output delays as we constrained by applying input delays in case of input signals.

If the data signals are constrained like this, the constraints can be applied at synthesis/implementation too as input/output delays are supported by all synthesis and implementation tools. Manual iterations are very few. On the other hand, for defining these checks, we need to have one reference clock. If we do not have a clock defined for the protocol, we cannot define these. Also, since regular setup and hold checks are also to be met, it becomes quite complex and confusing to calculate the amount of min and max delays to be applied.

Although the range of input and output setup times is fixed, there needs to be made some adjustments within this range, based upon the path delays and placement of the protocol logic inside the SoC. As in min/max delay, due to delay variations across PVTs, these checks need to be adjusted for different PVTs.

**Applying setup/hold checks**

The most effective way for constraining the signals with respect to maintaining a skew between them is to apply data checks between them. According to the definition of data-to-data check, it is applied between two signals, neither of which is a clock. Here, we can consider one of the signals as a reference and define other signal’s relationship with respect to it. The port having the reference signal becomes ‘reference port’ whereas the other port, i.e. the port which is constrained, becomes the ‘constrained port’. This method is different from the method described above in the sense that we do not need to define the reference data as a clock here.

Data check is similar to normal setup/hold check. An important difference is that data check is performed on the same edge as the launch flop (in normal setup check, capture edge is one edge away from launch edge). That is why, data to data checks are known as ‘zero cycle checks’.

A data-to-data check may be specified using ‘set_data_check’ command in EDA tools.

\[
\begin{align*}
\text{set_data_check} & \ -\text{from} \ <\text{reference_port}> -\to <\text{constrained_port}> \ <\text{value}> -\text{setup/-hold}
\end{align*}
\]

To constrain the signals for minimum skew requirement, we can simply apply data-to-data setup check (to constrain reference port to come later) or data-to-data hold check (to constrain the reference signal to come earlier), since data-to-data setup check is zero cycle – see figure 6.

To constrain the reference signal to come later,

\[
\begin{align*}
\text{set_data_check} & \ <\text{skew_requirement}> -\text{from} <\text{reference_signal}> -\to <\text{constrained_signal}> -\text{setup}
\end{align*}
\]

To constrain the reference signal to come earlier,

\[
\begin{align*}
\text{set_data_check} & \ <\text{skew_requirement}> -\text{from} <\text{reference_signal}> -\to <\text{constrained_signal}> -\text{hold}
\end{align*}
\]

On the contrary, to constrain the signals to be within a window, both setup and hold checks need to be applied – see figure 7. Also, the values to be applied have to be negative. In addition, a multicycle of -1 for hold needs to be applied.

The combination of commands to be applied is as follows:

\[
\begin{align*}
\text{set_data_check} & \ <\text{skew_requirement}>/2 -\text{from} <\text{reference_signal}> -\to <\text{constrained_signal}> -\text{setup} \\
\text{set_data_check} & \ <\text{skew_requirement}>/2 -\text{from} <\text{reference_signal}> -\to <\text{constrained_signal}> -\text{hold} \\
\text{set_multicycle_path} & \ -1 -\to <\text{constrained_port}> -\to <\text{reference_port}> -\text{hold}
\end{align*}
\]

Constraining the signals for skew requirement using data-to-data checks has several merits. As mentioned above, it is the simplest way to apply these types of constraints. Only relative skew between the signals matters while the signals themselves may have any value of delay. Unlike input/output delay method, there is no need for a clock to be present and the window requirement does not need to be updated across corners. However, uncertainty and derate values need to be taken into account, if applied.

Though data-to-data checks provide a robust and efficient way to apply these constraints, still there is some scope of improvement. Like it does take into account the uncertainties and derate, whereas the requirements specified are without any uncertainties and derates. So, we have to either make these windows larger taking into account uncertainties and derates; or we need to have support in EDA tools for path based derates and uncertainties.
**Revised IEEE 1149.1 ‘JTAG’ standard should reduce IC design costs through test re-use**

IEEE has released the revised IEEE 1149.1-2013 “Standard for Test Access Port and Boundary-Scan Architecture” (JTAG). This revision is intended to dramatically lower electronics industry costs by enabling test re-use across all phases of the integrated circuit lifecycle via vendor-independent, hierarchical test languages. The revision of IEEE 1149.1, the first for the standard since 2001, allows critical domain expertise for intellectual property (IP)—how to configure a serializer/deserializer (SERDES) for backpanel testing, for example—to be transferred in a computer-readable format from the IP designer to IC designers and, in turn, to designers of printed circuit boards (PCBs) and to test engineers, gradually magnifying industry cost savings along the supply chain. The cost savings for the electronics industry that IEEE 1149.1-2013 is intended to unlock are estimated to be in the billions of dollars. IEEE 1149.1-2013 specifies a new hierarchical Procedural Definition Language (PDL)—a standard test language based on Tcl, and hierarchical extensions to the original Boundary Scan Description Language (BSDL) to describe on-chip IP test data registers. Eight new optional IC instructions provide a foundation for configuring I/Os for board test, mitigating false failures when re-testing the IC at the board level and correlating the results back to wafer level test through an Electronic Chip ID. Now, the IP provider can document the IP test Interface and how to operate the IP in an English-like language—just once, for all ICs. Software tools then re-target this documentation at the IC and board level for tests. In revising IEEE 1149.1, the working group focused on two things: lowering industry costs through the new PDL language and enabling test re-use over the lifecycle of an integrated circuit. IEEE 1149.1-2013 provides critical synergy with two other important industry standards. IEEE 1149.1-2013 supports segmented on-chip test data registers that cross power domains specified by IEEE 1801-2013 “Standard for Design and Verification of Low Power Integrated Circuits”. IEEE 1149.1-2013 enables descriptions and operation of IP accessible via IEEE 1500-2005 “Standard Testability Method for Embedded Core-based Integrated Circuits” structures.

IEEE
www.ieee.org

**System builder design tool targets ARM-based SmartFusion2 SoC FPGAs**

Microsemi’s System Builder is a new design tool within the Libero System-on-Chip (SoC) Design Environment version 11.0 and is specifically targeted at accelerating customer definition and implementation of ARM-based systems using SmartFusion2 SoC FPGAs. The output from System Builder is automatically generated and correct-by-construction, thus eliminating the errors that are created when the architecture is specified ‘by hand’ as in more traditional tool flows. Thus, System Builder dramatically shortens the design cycle time for complex SoC FPGAs. Additionally, software-oriented engineers can easily create an embedded architecture and begin code development all on their own. This simplifies the adoption of Microsemi SmartFusion2 devices and provides a much broader set of design engineers with access to SoC FPGA technology. System Builder users are guided step-by-step through each of the main SoC FPGA architecture blocks. The design process uses a high-level graphical Interface that reacts to previous architecture selections and guides the user through the process of selecting options and configuring only the required embedded system blocks. The resulting system specification is automatically generated and correct-by-construction. It includes both the configuration and interconnects of the ARM processor and its related peripherals as well as other IP blocks implemented in the FPGA fabric. System Builder can also configure a growing set of IP blocks for high-performance interfaces including DDR2/DDR3/LPDDR memory controllers, and serial interfaces using 5Gbps SERDES for PCIe, XAU1 (10 GbE) and SGMII. Additional fabric-based parameterized IP functions available within System Builder include I2C, SPI, Timers, UARTs and PWM blocks. SmartFusion2 integrates inherently reliable flash-based FPGA fabric, a 166MHz ARM Cortex-M3 processor, advanced security processing accelerators, DSP blocks, SRAM, eNVM and industry-required high performance communication interfaces.

Microsemi
www.microsemi.com

**Debug probe supports Infineon’s single-pin debug interface**

Segger has added support for Infineon’s Single Pin Debug (SPD) Interface for Infineon’s XMC1000-series to the J-Link family of debug probes. The J-Link is, Segger asserts, the only commercial debug probe in the market capable of connecting to a device with the SPD-interface. “Support for Infineon’s SPD-interface makes J-Link even more versatile,” according to Segger, “We are making sure our complete line of J-Link debug probes support all major tool vendors, CPU architectures and target interfaces [and] the first vendor supporting Infineon’s XMC1000 series singlewire debug Interface is just one more point of proof”. “The SEGGER support for the SPD-interface significantly improves the eco-system for the XMC1000-series. By working with SEGGER, the SPD-interface is now accessible from all popular tool-chains in the market, including the free DAVE development platform and other free GDB-based development environments,” says Dr. Stephan Zizala, Senior Director, Industrial and Multimarket Microcontrollers at Infineon Technologies. The SEGGER J-Link debug probe on the market is tool chain independent and works with commercial IDEs from: Atmel, Atollic, Coocox, Freescale, IAR, i-Systems, ImageCraft, KEIL, Mentor Graphics, Phyton, Rowley, Renesas, Tasking and others, as well as free GDB-based tool chains such as emlDE and EmBlocks. J-Link supports multiple CPU families, such as ARM 7, 9, 11, Cortex-M0, M0+, M1, M3, M4, R4, A5, A8, A9 as well as Renesas RX610, 620, 62N, 62T, 630, 631, 63N; there is typically no need to buy a new J-Link or new license when switching to a different CPU family or toolchain.

Segger
www.segger.com/jlink.html

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Segger
www.segger.com/jlink.html
Overview

Get Ready to See a New World of 8-bit PIC® Microcontrollers
PIC microcontrollers are finding their way into new applications like solar battery chargers, advanced medical devices and solid state lighting. Microchip provides solutions for the entire performance range of 8-bit microcontrollers, with easy-to-use development tools, complete technical documentation, design-in and production support through a global sales and distribution network.

The Industry’s Broadest MCU Offering
There are over 800 8-bit PIC microcontrollers ranging from 6 to 100 pins and up to 128 KB Flash that are pin and code compatible across the portfolio. PIC microcontrollers with XLP technology feature the world’s lowest active and sleep power consumption with flexible power modes and wake-up sources. MPLAB® X Integrated Development Environment (IDE) supports all PIC microcontrollers with XC Compiler support and common development boards.

Peripherals, Performance, and Price Points for any Application
Peripheral integration is key with communication and control peripherals like SPI, I²C™, UART, PWM, ADC, DAC, op amps, as well as specialized peripherals for USB, LCD and Ethernet. In addition, Microchip offers the Core Independent Peripherals that provide even higher levels of flexibility and integration which has never been possible in the 8-bit microcontrollers. These new Core Independent Peripherals include Configurable Logic Cell (CLC), Complementary Output Generator (COG), Numerically Controlled Oscillator (NCO), Zero Cross Detect (ZCD) and Hardware CVD (Capacitive Voltage Divider). Customers have made PIC MCUs a worldwide standard, with over one million development systems shipped. PIC microcontrollers are quick and easy to design into a wide variety of applications with a long history of dependable product delivery.

Scalability & Migration
To provide customers a low-risk development environment, PIC microcontrollers offer seamless migration within the complete range of products. The 8-bit PIC microcontroller family is pin-compatible within a given pin count as well as code compatible between the architectures. Being able to migrate easily between various PIC MCUs allows flexibility to react to changing design requirements and feature enhancements. Maximize re-use for future developments and preserve the investment in hardware, software and tools by choosing Microchip.

Strength Through Design
In an effort to meet the needs of embedded system designers, silicon manufacturers continue to increase functionality and performance while decreasing the physical size and cost. This provides a significant benefit to both the embedded system designer and end consumer, but as the demand for sophisticated consumer and embedded products continues to expand, so does the challenge of properly designing such applications.

As semiconductor technology continues to evolve into “smaller, faster and cheaper”, so does the challenge to provide key features and attributes necessary for embedded design. Microchip is committed to implementing technology advances that not only increase performance and reduce cost of the microcontroller, but do so without sacrificing key features such as:

- **5V**: As an 8-bit leader, we understand the need for 5V devices and will continue to support it.
- **EEPROM**: A key requirement for many embedded designs, cost effective implementation is critical.
- **Analog Integration**: Having a rich Analog offering available in a low cost MCU is a must have for many of today’s embedded challenges.
- **High Voltage Variants**: Allows for connection to an application that has high voltage rails, without the need of an external regulator.
- **EMC**: Designed to minimize susceptibility to EMI/EMC, providing the most electrically durable solutions in the industry.
Global Support
Microchip provides 24/7 global technical support with on-line and phone support, hundreds of dedicated field application engineers, more than 50 sales offices and our authorized distributor network. Microchip also offers standard code libraries, reference designs, application notes and seminars on-line and at Microchip Regional Training Centers.
www.microchip.com/8bitresources

Trusted partner
While MCU core commonality is a trend, there are no “drop in” replacements. The reality of MCU selection is that you are entering into a partnership with your MCU supplier. To ensure success, technology leadership is critical, but it is equally important to work with a partner that is committed to strong business fundamentals such as:
- Financial security to weather any economic downturns
- Industry leading lead times
- Industry leading quality and reliability (ISO/TS-16949 qualified)
- Industry leading EOL policy

8-bit PIC Microcontroller Key Highlights

Core Independent Peripherals
- Configurable Logic Cell (CLC)
- Complementary Waveform/Output Generator (CWG/COG)
- Numerically Controlled Oscillator (NCO)
- Programmable Switch Mode Controller (PSMC)

Intelligent Analog
- Rail-to-rail op amps
- Fast comparators
- 12b/10b/8b ADC
- 9b/8b/5b DAC
- Zero Cross Detect (ZCD)
- Voltage reference

Small Form Factors
- As small as 8-pin 2 × 3 UQFN and 28-pin 4 × 4 UQFN
- Many other package options available, e.g. 3 × 3 QFN, 5 × 5 UQFN

eXtreme Low Power (XLP)
- Active current as low as < 30 µA/MHz
- Sleep current as low as < 10 nA
- Battery lifetime > 20 years

Essential Features
- 5V+ operation
- EEPROM
- LCD, mTouch™ Sensing Solutions
- USB, CAN, Ethernet
- Analog Integration

Faster Time-to-Market
- Free software
- Pin and code compatibility, easy migration
- Pre-programmed parts via Quick Turn Programming (QTP)

Design Support
- Free MPLAB® X Integrated Development Environment
- Free C Compilers
- Comprehensive technical documentation
- World-class, 24/7 technical support and training

8-bit PIC® Microcontroller Solutions
8-bit PIC MCU Architectures

Unified MPLAB Tool Suite/XC8 Compiler
Free IDE • Free C Compilers • Free Software Libraries

Architecture:

Baseline
5 MIPS
0.375–3 KB Flash
6–40 Pins

Mid-Range
5 MIPS
0.48–14 KB Flash
6–64 Pins

F1 Enhanced Mid-Range
8 MIPS
1.75–28 KB Flash
8–64 Pins

PIC18
16 MIPS
4–128 KB Flash
Hardware Multiplier
18–100 Pins

Family:

<table>
<thead>
<tr>
<th></th>
<th>Baseline Architecture</th>
<th>Mid-Range Architecture</th>
<th>F1 Enhanced Mid-Range Architecture</th>
<th>PIC18 Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>Families</td>
<td>PIC10, PIC12, PIC16</td>
<td>PIC10, PIC12, PIC16</td>
<td>PIC12F1, PIC16F1</td>
<td>PIC18</td>
</tr>
<tr>
<td>Pin Count</td>
<td>6-40</td>
<td>6-64</td>
<td>8-64</td>
<td>18-100</td>
</tr>
<tr>
<td>Interrupts</td>
<td>No</td>
<td>Single interrupt capability</td>
<td>Single interrupt capability with hardware context save</td>
<td>Multiple interrupt capability with hardware context save</td>
</tr>
<tr>
<td>Performance</td>
<td>5 MIPS</td>
<td>5 MIPS</td>
<td>8 MIPS</td>
<td>Up to 16 MIPS</td>
</tr>
<tr>
<td>Instructions</td>
<td>33, 12-bit</td>
<td>35, 14-bit</td>
<td>49, 14-bit</td>
<td>83, 16-bit</td>
</tr>
<tr>
<td>Program Memory</td>
<td>Up to 3 KB</td>
<td>Up to 14 KB</td>
<td>Up to 28 KB</td>
<td>Up to 128 KB</td>
</tr>
<tr>
<td>Data Memory</td>
<td>Up to 134B</td>
<td>Up to 368B</td>
<td>Up to 1.5 KB</td>
<td>Up to 4 KB</td>
</tr>
<tr>
<td>HardwareStack</td>
<td>2 level</td>
<td>8 level</td>
<td>16 level</td>
<td>32 level</td>
</tr>
<tr>
<td>Features</td>
<td>Comparator</td>
<td></td>
<td>In addition to Baseline:</td>
<td>In addition to Enhanced Mid-Range:</td>
</tr>
<tr>
<td></td>
<td>8-bit ADC</td>
<td></td>
<td>SPI/IPC™, UART, PWMs, LCD, 10-bit ADC, Op amp, Configurable logic cells, Numerically controlled oscillator, Complementary waveform generator, Hardware CVD, High speed comparators</td>
<td>8 x 8 Hardware multiplier, CAN, CTMU, Ethernet</td>
</tr>
</tbody>
</table>

Continuous development across all architectures and families.
Core Independent Peripherals

Summary
The following Core Independent Peripherals take 8-bit MCU performance to a new level, while requiring no processor overhead.

- **CLC (Configurable Logic Cell)**: The CLC provides programmable combinational and sequential logic. It also enables on-chip interconnection of peripherals and I/O, thereby reducing external components, saving code space, and adding functionality.

- **NCO (Numerically Controlled Oscillator)**: A programmable precision linear frequency generator, ranging from <1 Hz to 500 KHz+. The NCO offers a step up in performance, and a simplification in design, for applications requiring precise linear frequency control, such as: fluorescent ballasts, lighting control, radio tuning circuitry, Class D audio amplifiers, etc.

- **Hardware CVD (Capacitive Voltage Divider)**: The Hardware CVD is a hardware implementation of our Capacitive Voltage Divider. It enables capacitive touch sensing and proximity detection while simplifying the design, reducing code size and decreasing CPU usage.

- **COG (Complementary Output Generator)/ CWG (Complementary Waveform Generator)**: The CWG provides a complementary waveform with rising and falling edge dead band control, enabling high efficiency synchronous switching, with no processor overhead. The CWG also incorporates auto shutdown, auto restart, and can directly interface with other peripherals/external inputs. The COG takes the CWG and improves its performance with blanking and phase control.

- **PSMC (Programmable Switch Mode Controller)**: The PSMC is a high performance 16-bit PWM with 6 configurable outputs that can operate in multiple modes. With a dedicated 64MHz clock and the flexibility to interface to external inputs as well as integrated peripherals/clock sources, the PSMC offers the highest level of advanced PWM control and accuracy in an 8-bit MCU. The PSMC can simplify the implementation of a wide array of applications such as: motor control, lighting, and power supplies.

### Development Tools

**PICkit Low Pin Count Development Board (DM164130-9)**
- Dev board for 8, 14, 20-pin 8-bit PIC® MCU
- Populated with PIC16F1829-I/P and ships with PIC18F14K22-I/P (20-pin) MCU
- This board package contains assembled board with area for prototyping circuits and bare board as well
- Software can be rewritten to accommodate new technologies

**PIC10F32X Development Board (AC103011)**
- Populated with the PIC10F322 6-pin MCU
- Factory programmed with CWG, NCO and CLC demo software
- Prototype area for development purposes
- User's guide and source code available

### Featured Core Independent Peripherals Product Families

<table>
<thead>
<tr>
<th>Family</th>
<th>Pins</th>
<th>Flash Memory SRAM (Bytes)</th>
<th>Capture Compare/ PWM</th>
<th>Analog</th>
<th>Core Independent Peripherals</th>
<th>Communications Serial I/O</th>
<th>Additional Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC10(L)F32X</td>
<td>6</td>
<td>448–896</td>
<td>0</td>
<td>8-bit ADC (3)</td>
<td>CLC, NCO, CWG</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>PIC16(L)F150X</td>
<td>8/14/20</td>
<td>1.75K–14K 64–512</td>
<td>0</td>
<td>10-bit ADC (4–12), 5-bit DAC (0–1), Comparators (1–2)</td>
<td>CLC, NCO, CWG</td>
<td>UART, I²C™/SPI</td>
<td>Fixed Voltage Ref</td>
</tr>
<tr>
<td>PIC12LF1552</td>
<td>8</td>
<td>2K</td>
<td>0</td>
<td>10-bit ADC (5)</td>
<td>HCVD</td>
<td>I²C/SPI</td>
<td>Fixed Voltage Ref</td>
</tr>
<tr>
<td>PIC16(L)F151X</td>
<td>28</td>
<td>2K–4K 128–256</td>
<td>2</td>
<td>10-bit ADC(17)</td>
<td>HCVD</td>
<td>UART, I²C/ SPI</td>
<td>Fixed Voltage Ref</td>
</tr>
</tbody>
</table>

www.microchip.com/cip

8-bit PIC® Microcontroller Solutions
Intelligent Analog

Summary
With Microchip’s Intelligent Analog solutions, engineers can reduce their component count, design smaller, more cost effective boards, and benefit from simplified, higher performance designs and easier procurement of components. In addition, designers benefit from increased flexibility like analog topology agility, utilizing the MCU’s programmable analog interconnects and programmability.

To simplify your next design, Microchip has integrated the following Analog Peripherals.

Op Amps
A basic building block in electronic design. Integrating op amps into the Microcontroller offers increased flexibility and reliability while reducing BOM costs and board space.

High Speed Comparators
Comparators have been in the PIC Microcontroller lineup for many years. We are now offering feature rich High Speed (50 nS) variants to enable faster responding/more efficient closed loop feedback designs.

Fixed Voltage Reference
Fixed Voltage Ref provides an integrated stable voltage reference, independent of VDD.

Analog to Digital Conversion
■ 16, 12, 10 and 8-bit ADCs available in our 8-bit offering

Digital to Analog Conversion
■ 9,8, and 5-bit DAC options available in our 8-bit offering

High Current Sink/Source Pins
High Current Sink/Source pins with the ability to sink/source 50 mA the high currents pins enable direct MOSFET drive from the microcontroller.

Zero Cross Detect
Enables the micro to be connected directly to the AC input via a current limiting resistor. The ZCD will flag the micro when the Zero Cross is approaching so any required switching can be synchronized to reduce power and eliminate any switching related artifacts/noise.

Development Tools
F1 PSMC 28-pin Evaluation Board (DM164130-10)
■ PSMC development platform using the PIC16F1783
■ Break-out headers for application development
■ Connect to any F1 motor control add-on
■ Prototyping area

PICDEM™ Lab Development Kit (DM163045)
■ Development platform for 6 to 20-pin parts
■ Work across different architectures
■ Includes comprehensive user guide, labs, and application examples
■ Support for PICkit™ 3 and Expansion Headers

Featured Intelligent Analog Product Families

<table>
<thead>
<tr>
<th>Family</th>
<th>Pins</th>
<th>Flash Memory SRAM (Bytes)</th>
<th>Intelligent Analog</th>
<th>Core Independent Peripherals</th>
<th>Additional Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC16F527/570</td>
<td>20/28</td>
<td>1.5K–3K 64–132</td>
<td>8-bit ADC (8), Comparator (2), Op amp (2)</td>
<td>-</td>
<td>Internal Shunt: providing high voltage input capability</td>
</tr>
<tr>
<td>PIC16F75X</td>
<td>8/14</td>
<td>1.75 KB–3.5 KB 64–128</td>
<td>10-bit ADC (4), 5/9-bit DAC (1), Comparators (2), Op amp (1), High Current Pins (2)</td>
<td>CWG/COG</td>
<td></td>
</tr>
<tr>
<td>PIC16(L)F170X</td>
<td>14/20</td>
<td>3.5 KB–14 KB 256 B–1 KB</td>
<td>10-bit ADC (8-12), 8-bit DAC (1), Op amps (2), Comparators (2), Zero Cross Detect</td>
<td>CLC,COG</td>
<td>I²C™/SPI, UART</td>
</tr>
<tr>
<td>PIC16(L)F171X</td>
<td>28/40/44</td>
<td>7 KB–28 KB 512–2 KB</td>
<td>10-bit ADC (17–28), 5 &amp; 8-bit DAC, Op amps (2), Comparators (2), Zero Cross Detect</td>
<td>CLC, NCO, COG</td>
<td>I²C/SPI, UART</td>
</tr>
<tr>
<td>PIC16(L)F178X</td>
<td>28/40/44</td>
<td>2K - 16K 256 - 2K</td>
<td>12-bit ADC (11–14), Comparators (3–4), Op amps (2–3), 8-bit DAC, 5-bit DAC (0–3)</td>
<td>PSMC</td>
<td>I²C/SPI, UART</td>
</tr>
</tbody>
</table>

www.microchip.com/intelligentanalog
eXtreme Low Power (XLP) Technology

- Sleep currents down to 9 nA
- Active Mode currents down to 30 µA/MHz
- Execution Efficiency with more than 80% PIC MCU single cycle instructions
- Execute code smarter, sleep longer, maximize battery life
- Wake-up sources including RTC, WDT, BOR, Interrupts, Reset or POR

Low Power Peripheral Integration

Many of today’s low power products need advanced peripherals. Microchip offers low power devices with peripherals like USB, LCD and mTouch capacitive sensing. This eliminates the need for additional parts in the application, which saves cost, current and complexity.

Low Power Reliability

In addition to peripherals, products with XLP have system supervisory circuits specially designed for battery powered products.
- Watchdog Timer down to 200 nA, provides protection against system failure
- Real-Time Clock/Calendar down to 400 nA, provides precise timekeeping
- Brown-out Reset down to 45 nA, protects as batteries are depleted or changed

Battery Life Estimator

The XLP Battery Life Estimator is a free software utility to aid you in developing eXtreme Low Power applications with Microchip’s PIC MCUs featuring XLP technology.
- Profile your application Run and Sleep time (duty cycle)
- Select operating temperature and operating voltage
- Pre-loaded with most common battery specifications
  www.microchip.com/XLP

Run from a Single Battery

The MCP1623/4 and MCP1640 Synchronous Boost Regulators enable single cell battery applications, ideal for small, portable and lightweight applications.
- Power any PIC MCU down to 0.35V
- Provides 2–5.5V fixed/stable output voltage

Development Tools

XLP 8-bit Development Board (DM240313)
- Supports PIC16 and PIC18 devices
- LCD display and buttons
- Flexible power options
- Expansion connector
- Current measurement points

Featured XLP Product Families

<table>
<thead>
<tr>
<th>Device Family</th>
<th>Pins</th>
<th>Flash (KB)</th>
<th>Sleep (nA)</th>
<th>Active (µA/MHz)</th>
<th>Special Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC16F727</td>
<td>20–44</td>
<td>3.5–14</td>
<td>20</td>
<td>55</td>
<td>–</td>
</tr>
<tr>
<td>PIC16F1509</td>
<td>20</td>
<td>7–14</td>
<td>25</td>
<td>30</td>
<td>CLC, CWG, NCO</td>
</tr>
<tr>
<td>PIC16F1829</td>
<td>8–20</td>
<td>3.5–14</td>
<td>20</td>
<td>50</td>
<td>–</td>
</tr>
<tr>
<td>PIC16F1947</td>
<td>28–64</td>
<td>7–28</td>
<td>60</td>
<td>55</td>
<td>LCD</td>
</tr>
<tr>
<td>PIC18F46K20</td>
<td>28–40</td>
<td>8–64</td>
<td>50</td>
<td>138</td>
<td>–</td>
</tr>
<tr>
<td>PIC18F87K22</td>
<td>20–80</td>
<td>8–128</td>
<td>20</td>
<td>190</td>
<td>–</td>
</tr>
<tr>
<td>PIC18F47J53</td>
<td>28–44</td>
<td>16–128</td>
<td>9</td>
<td>197</td>
<td>USB</td>
</tr>
<tr>
<td>PIC18F66K80</td>
<td>28–64</td>
<td>32–64</td>
<td>13</td>
<td>100</td>
<td>CAN</td>
</tr>
<tr>
<td>PIC18F87K90</td>
<td>64–80</td>
<td>32–128</td>
<td>20</td>
<td>180</td>
<td>LCD</td>
</tr>
</tbody>
</table>

All numbers are typical values, sleep numbers refer to the lowest power sleep mode available on each family.

www.microchip.com/xlp
Touch Sensing
Touch sensing has become an alternative to traditional push-buttons and switches providing:
- Lower cost of manufacturing and assembly
- Elegant and stylish designs
- Increased reliability; with fewer moving parts
- Proximity-sensitive human interfaces

Microchip’s mTouch Sensing Solutions allow designers to integrate touch sensing with application code in a single microcontroller, reducing total system cost. Microchip offers a broad portfolio of low power, low cost and flexible solutions for keys/sliders and touch screen controllers. Get to market faster using our easy GUI-based tools, free source code and low-cost development tools.

Keys, Sliders, Wheels and Proximity Detection
- Industry’s lowest power touch sense solutions
  - Capacitive sensing in less than 5 μA
  - Proximity sensing down to less than 1 μA
- No external component
- Works through plastic, glass and metal surfaces
- Water-proof designs for all weather conditions
- High noise robustness
- Integrated peripherals such as USB, segmented and graphical LCD modules for true human interface system on a chip
- Free software library simplifies implementation and source code puts you in control

Capacitive Voltage Divider (CVD)
CVD is a charge/voltage based technique to measure relative capacitance on a pin using only the ADC.
- Software implementation
- 8, 16, and 32-bit support
- Proximity support
- Low temperature dependence
- Low VDD dependence
- Minimal hardware requirements
- Low-frequency noise rejection
- Metal over cap compatible

Hardware CVD
Hardware CVD has been implemented on some of our new devices providing automated capacitive touch sampling, thereby reducing code size and decreasing CPU usage.

Development Tools
Enhanced mTouch Technology Capacitive Evaluation Kit (DM183026-2)
- Features PIC16F, PIC18F, PIC24F and PIC32F
- Includes 8 buttons, matrix and sliders daughter boards
- GUI for easy configuration and real time data monitoring

mTouch Projected Capacitive Development Kit (DM160211)
- PIC16F707 controller board with fully functional firmware
- Sensor board with 3.5” projected capacitive 12 × 9 touch screen
- Royalty-free source code supports sensors with up to 32 channels

Metal Over Cap Accessory Kit (AC183026)
- For use with the DM183026-2
- 1 daughter board featuring stainless steel cover
- 1 daughter board featuring a plastic cover

Featured HCVD Product Families

<table>
<thead>
<tr>
<th>Device Family</th>
<th>Pins</th>
<th>Flash (KB)</th>
<th>HCVD</th>
<th>Voltage (V)</th>
<th>Additional Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC16LF1513</td>
<td>28</td>
<td>2–4</td>
<td>✓</td>
<td>1.8–5.5</td>
<td>10-bit ADC × 17 channels, CCPWM, UART, I²C™, SPI</td>
</tr>
<tr>
<td>PIC12LF1552</td>
<td>8</td>
<td>2</td>
<td>✓</td>
<td>1.8–3.6</td>
<td>10-bit ADC × 5 channels I²C, SPI</td>
</tr>
</tbody>
</table>

Software CVD available on all PIC MCUs with ADC
Segmented Displays
Segmented displays are used in a wide variety of applications, ranging from meters to portable medical devices to thermostats to exercise equipment. PIC MCUs with integrated LCD drivers can directly drive segmented displays with letters, numbers, characters and icons. The main features of Microchip’s LCD portfolio include:

- Flexible LCD segments
  - 28 pins: up to 72 segments
  - 44 pins: up to 116 segments
  - 64 pins: up to 184 segments
  - 80 pins: up to 192 segments
  - 100 pins: up to 480 segments
- Variable clock inputs
- Integrated voltage bias generation
- Direct drive for both 3V and 5V powered displays
- Software contrast control for boosting or dimming for different temperature or lighting conditions
- Drive LCD while conserving power in Sleep mode
- Integrated real time clock and calendar for displaying time and date information
- ATtiny capacitive touch sensing capability
- Crystal-free USB 2.0 options

Direct Drive for Segmented Displays
The LCD PIC microcontrollers support direct LCD panel drive capability with no external components needed, lowering total system cost. They have integrated voltage bias generation which allows the MCU to generate the different voltage levels that are required to drive the LCD segment pins and provide good contrast for the display. The LCD MCUs support a range of fixed and variable bias options as well as variable clock inputs that enable the flexibility to work with many different glass vendors.

Contrast Control
Software contrast control is a key feature using firmware to either boost or dim the contrast of the display. Boost the contrast up to VDD or beyond if you are using one of the MCUs with an integrated charge pump. Software contrast control allows the designer to vary the contrast on the LCD to account for different operating conditions such as temperature, lighting, and humidity. Also, software contrast control can be invaluable for portable applications. As the battery level starts to drop, the firmware can apply a boost to the contrast helping extend the battery life while still seeing a crisp image on the display.

Development Tools

**PICDEM™ LCD 2 Demo Board (DM163030)**
- Illustrates and supports the main features of Microchip’s 28-, 40-, 64- and 80-pin LCD PIC microcontrollers
- LCD glass with icons, numbers, alphanumeric and starburst display
- Separate Processor Plug-in Modules (PIMs) are available to evaluate all of the LCD products
- Booster capability for contrast control and dimming

**LCD Explorer Development Board (DM240314)**
- Supports PIC24 & PIC18 LCD PIC MCUs with XLP technology
- Current measurement terminals, mTouch sensing solutions & expansion connector

**PIC18F97J94 PIM Demo Board (MA180034)**
- Features 100-pin PIC18F97J94 for evaluation of all 100-, 80- and 64-pin PIC18F97J94 LCD/USB/General Purpose MCUs
- Plugs into LCD Explorer Board (DM240314) for additional functionality
- Contains code examples

**Featured LCD Product Families**

<table>
<thead>
<tr>
<th>Device Family</th>
<th>Pins</th>
<th>Flash (KB)</th>
<th>Max Segments</th>
<th>Voltage (V)</th>
<th>Additional Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC16LF1907</td>
<td>28–40</td>
<td>3.5–14</td>
<td>116</td>
<td>1.8–3.6</td>
<td>10-bit ADC, EUSART</td>
</tr>
<tr>
<td>PIC16LF1947</td>
<td>28–64</td>
<td>7–28</td>
<td>184</td>
<td>1.8–5.5</td>
<td>10-bit ADC, EEPROM, I²C™, SPI, Comparators</td>
</tr>
<tr>
<td>PIC18F87K90</td>
<td>64–80</td>
<td>32–128</td>
<td>192</td>
<td>1.8–5.5</td>
<td>10-bit ADC, EEPROM, I²C, SPI, RTCC, Comparators, ECCP</td>
</tr>
<tr>
<td>PIC18F97J94</td>
<td>64–100</td>
<td>32–128</td>
<td>480</td>
<td>2–3.6</td>
<td>Crystal-free USB, VDD, 12-bit ADC, ECCP, UART, I²C, SPI, Comparators</td>
</tr>
</tbody>
</table>

**www.microchip.com/lcd**

8-bit PIC® Microcontroller Solutions 9
PIC Microcontrollers with Integrated USB

USB
USB communication is growing in popularity for remote upgrades, downloading data and other portable serial communication applications. Microchip's USB PIC MCUs bring the benefits of full-speed USB to a broad range of embedded designs that can operate in various environments and locations, enabling easy access to other USB devices such as printers, handheld devices or PCs.

Full-Speed USB 2.0 (Device)
Microchip offers USB solutions capable of full-speed USB operation with the PIC16 and PIC18 family of devices. If USB On-The-Go is a requirement we have solutions in our 16 and 32 bit families.

Crystal-Free USB
USB communication requires 48 MHz with 0.25% accuracy over temperature. This is typically done with an external crystal and an internal USB. We have recently implemented technologies that allow a crystal-free implementation with the following benefits:
- Lower BOM cost
- Tiny PCB footprint
- Simplified design
- More robust solution

Free USB Software
Microchip has USB software to support USB on 8, 16 and 32-bit MCUs. This software is royalty-free source code and also includes sample projects. The 8-bit family supports USB device mode with full speed operation. Additional software support includes full C and RTOS development environments. Included within this USB Framework Library is Microchip’s USB Framework Configuration Tool.
- Generates configuration files with just a few clicks
- Royalty-free source code
- Firmware projects and USB drivers for the PC

Add USB to any PIC MCU with UART
The MCP2200 is a stand-alone USB to UART serial converter that enables full-speed USB connectivity in applications containing a UART interface. The MCP2200 has 256 bytes of EEPROM and 8 general purpose I/O.
It offers a simple “plug-and-play” solution, allowing USB connectivity with very little design effort.

Development Tools
Low Pin Count USB Development Kit (DV164139/DM164127)
- Development platform for 14 and 20-pin USB MCUs
- For evaluation of PIC18F14K50/13K50 20-pin USB MCUs + 145X
- Contains hardware, software and code examples
- Self-directed course and lab materials

PICDEM Full-Speed USB Demo Kit (DM163025-1)
- Evaluation platform for PIC18F2X/4XK50 family of USB MCUs
- Full speed USB 2.0 device without the need for an external crystal
- Populated with the PIC18F45K50

PIC18F87J94 PIM Demo Board (MA180033)
- Features 80-pin PIC18F87J94 MCU for evaluation of all 80- and 64-pin PIC18F97J94 USB/LCD/General Purpose MCUs
- Can be used with PIC18 Explorer Board (DM183032) for additional functionality
- Contains code examples

Featured Crystal-Free Product Families

<table>
<thead>
<tr>
<th>Device Family</th>
<th>Pins</th>
<th>Flash (KB)</th>
<th>Voltage (V)</th>
<th>Crystal-Free</th>
<th>Additional Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC16(L)F1459</td>
<td>14–20</td>
<td>7–14</td>
<td>1.8–5.5</td>
<td>✔</td>
<td>CWG, 10-bit ADC, DAC, µC™, SPI, UART</td>
</tr>
<tr>
<td>PIC18(L)F45K50</td>
<td>28–44</td>
<td>16–32</td>
<td>1.8–5.5</td>
<td>✔</td>
<td>10-bit ADC, Comparators, ECCP, UART, SPI, µC</td>
</tr>
<tr>
<td>PIC18F97J94</td>
<td>64–100</td>
<td>32–128</td>
<td>2–3.6</td>
<td>✔</td>
<td>VBat, 12-bit ADC, LCD, ECCP, UART, PIC, SPI, Comparators</td>
</tr>
</tbody>
</table>

www.microchip.com/usb
PIC Microcontrollers with Ethernet

**Embedded Ethernet**
Microchip addresses the growing demand for embedded Ethernet products with the ENC624J600, ENC424J600 and ENC28J60 as standalone Ethernet controllers, and the PIC18F97J60 family, which are IEEE 802.3™ compliant and fully compatible with 10/100/1000 Base-T networks. Microchip’s Ethernet solution also includes: Free and robust TCP/IP stack optimized for PIC microcontroller and dsPIC® digital signal controller families (www.microchip.com/tcpip).

**Development Tools**

**PICDEM.net™ 2 Development Board (DM163024)**
- Supports ENC28J60 and PIC18F97J60 devices
- Can be developed as web server

**PICI™ Ethernet Daughter Board (AC164121)**
- Can be plugged to any of the PIC18 demonstration boards
- Populated with ENC28J60
- Interfaces to RJ-45 female connector

---

PIC Microcontrollers with CAN & LIN

**Controller Area Network (CAN)**
Microchip offers a complete line of 8-, 16- and 32-bit MCUs to meet the needs of high-performance, embedded applications using the CAN bus. On-chip peripherals include A/D converters, comparators, motor control PWMs, USART (RS485, RS232, LIN) and Master I²C/SPI.

**Microchip’s Enhanced CAN Module**
- Supports CAN 1.2, CAN 2.0A and CAN 2.0B protocols
- DeviceNet data bytes filter support
- Standard and extended data frames
- 0–8 bytes data length
- Three modes of operation:
  - Mode 0: Legacy mode
  - Mode 1: Enhanced Legacy mode with DeviceNet support
  - Mode 2: FIFO mode with DeviceNet support
- Six buffers programmable as Rx/Tx buffers

**Local Interconnect Network (LIN)**
Microchip offers a LIN compatible USART on a wide variety of microcontrollers. We have recently taken our LIN offering to a new level by offering microcontrollers with integrated LIN transceivers.

**Development Tools**

**PICDEM CAN-LIN 3 Demonstration Board (DM163015)**
- Demonstrates CAN module features
- Includes both firmware and PC software for simulating a CAN network
- In addition, the board employs a LIN sub-network

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**Featured CAN & LIN Product Families**

<table>
<thead>
<tr>
<th>Device Family</th>
<th>Pins</th>
<th>Flash (KB)</th>
<th>CAN Tx Buffers</th>
<th>CAN Rx Buffers</th>
<th>LIN Tx Rx</th>
<th>Voltage (V)</th>
<th>Additional Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC18F4685</td>
<td>28–44</td>
<td>16–96</td>
<td>3</td>
<td>2</td>
<td>–</td>
<td>2–5.5</td>
<td>LIN USART</td>
</tr>
<tr>
<td>PIC18F66K80</td>
<td>28–64</td>
<td>32–64</td>
<td>3</td>
<td>2</td>
<td>–</td>
<td>1.8–5.5</td>
<td>LIN USART</td>
</tr>
<tr>
<td>PIC16F1829LIN</td>
<td>14</td>
<td>8K</td>
<td>–</td>
<td>–</td>
<td>Integrated</td>
<td>2.3–5.5</td>
<td>LIN USART</td>
</tr>
</tbody>
</table>

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www.microchip.com/can
www.microchip.com/lin
Support
Microchip is committed to supporting its customers in developing products faster and more efficiently. We maintain a worldwide network of field applications engineers and technical support ready to provide product and system assistance. In addition, the following service areas are available at www.microchip.com:

- **Support** link provides a way to get questions answered fast: http://support.microchip.com
- **Sample** link offers evaluation samples of any Microchip device: http://sample.microchip.com
- **Forum** link provides access to knowledge base and peer help: http://forum.microchip.com
- **Buy** link provides locations of Microchip Sales Channel Partners: www.microchip.com/sales

Training
If additional training interests you, then Microchip can help. We continue to expand our technical training options, offering a growing list of courses and in-depth curriculum locally, as well as significant online resources – whenever you want to use them.

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- **Worldwide Seminars**: www.microchip.com/seminars
- **eLearning**: www.microchip.com/webseminars
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11/27/12

Microcontrollers • Digital Signal Controllers • Analog • Memory • Wireless

www.microchip.com
EDA tool optimises cell libraries for processor cores in SoCs

Synopsys has announced a physical-IP design kit optimised for SoC processor cores; the DesignWare HPC Design Kit yields superior performance, power and area for CPU, GPU and DSP Cores. Synopsys has announced an extension to its DesignWare Duet Embedded Memory and Logic Library IP portfolio specifically designed to enable the optimised implementation of a broad range of processor cores. The new DesignWare HPC (High Performance Core) Design Kit contains a suite of high speed and high density memory instances and standard cell libraries that allow system on chip (SoC) designers to optimise their on chip CPU, GPU and DSP IP cores for maximum speed, smallest area or lowest power – or to achieve an optimum balance of the three for their specific application. Synopsys developed in collaboration with partners including Imagination Technologies, CEVA and VeriSilicon. The tool operates in conjunction with the synthesis stage of a design flow (in a flow where the synthesis is aware of floorplanning issues), and is in part empirical; based on studies of “what works best” when implementing logic structures typical of processor cores, it selects and lays down specific standard cell variants when it recognises certain features of processor logic, improving speed, power and silicon area. It includes around 125 new cells and memory elements. Initially focused on TSMC’s 28-nm HPM process, Synopsys says it will produce variants for other processes at that node, including low-power versions; 16-nm fin-FET processes are a further possible target, and the company “may” look back at 40-nm processes if demand exists. The optimisation package uses standard “Liberty” syntax.

Synopsys

www.synopsys.com/hpc-ip

System planner tool automatically generates 3D mechanical constraints

Zuken has released new versions of its System Planner and Design Gateway engineering solutions that accelerate and streamline product planning and logical design for engineers. System Planner includes new functions that allow design architects to study behaviour, signal quality, and 3D space constraints. Design Gateway includes improvements for hierarchy, rule checking, and an Schematic Connectivity Format (ISCF) format for Intel design review. Zuken has streamlined the design flow for real-world engineering design, embedding multi-board SI analysis into System Planner. This permits engineers to study behaviour and signal quality of system-level interconnections during the early design planning stage. It also facilitates “what-if” analysis to capture optimal topology and termination schemes earlier in the design process. Additionally, by importing accurate 3D enclosure and component models, engineers can create board outlines, see component profiles, and automatically generate mechanical constraints (such as height restrictions) for multi-board floor planning. Enhanced design reuse supports drag-and-drop of logical and physical data from the reuse library directly in System Planner. These can be fed directly into the design flow with Design Gateway (logical design) and Design Force (physical design). Design Gateway’s Circuit Advisor, part of Zuken’s schematic engineering environment, includes new rule checks to support multi-board design for physical connector mismatch, and physical data to reuse library directly in System Planner. These include new I/O checks to ensure proper continuity between boards, and checks for duplicate references throughout the system. Simplified classification of nets and constraint entry allow users to define complex spacing requirements for High-Speed interfaces such as PCI Express and DDR2/3/4.

Zuken

www.zuken.com

Automated software-driven verification tool

Vayavya Labs has released SOCX-Verifier, claimed to be the EDA industry’s first software-driven verification tool that automatically generates verification test software and relevant test-bench components from a system-level scenario specification.

With SOCX-Verifier, SoC designers can now bridge and greatly accelerate the arduous hardware-software co-design process. While there are flows that are based on virtual platforms and emulation platforms, there is still a huge amount of effort and cost involved in developing embedded software for SoCs. SOCX-Verifier provides all the necessary building blocks for driver-model generation, scenario specification and virtualizing test-bench interaction to give verification teams a speedier closure and effective system-level verification. Further this also enables the software developers to deliver production ready software drivers at a 10x efficiency level, according to Vayavya Labs. Software-driven verification methodology harnesses the embedded processor core’s power to verify the SoC from “Inside-Out.” SOCX-Verifier provides verification designers with the required infrastructure and building blocks for driver-model generation, scenario specification and virtualizing test-bench interaction for a speedier closure and effective system-level verification. It consists of two main components: SOCX-Specifier and SOCX-Virtualizer. SOCX-Specifier brings the canvas for capturing the scenario specifications and generates C test cases from this specification. The C test cases execute on the embedded processor core(s) in the SoC and access the design-under-test (DUT) components (design IP blocks) and the test-bench. SOCX-Virtualizer virtualizes access to the DUT components as well as the test-bench across various verification platforms. It achieves this by means of a “verification aware” lightweight operating system (OS) and the DDGen tool which automatically generates device drivers for the DUT components.

Vayavya Labs

www.vayavyalabs.com
Multiprocessing software tools target the CommAgility DSP board

3L Ltd, a provider of software tools to simplify multiprocessing, has released the 3L Diamond suite for use with the CommAgility AMC-2C6678 high performance DSP/FPGA card. 3L Diamond auto-magically handles the interconnection management when tasks are moved to different cores or devices. Engineers are free to focus on the application instead of the irritating minutiae of the connectivity. This freedom helps maximise the benefits of the C6678 multicore DSPs from Texas Instruments Incorporated (TI), built on the KeyStone architecture. The AMC-2C6678 is a single-width, full-sized AMC card powered by two of TI's latest TMS320C6678 DSPs, each with eight 1.25GHz C66x cores. The board also includes a Xilinx Virtex-6 FPGA and a 20Gbps per port Serial RapidIO infrastructure. The CommAgility AMC-2C6678 is the latest of many pre-installed hardware platforms supported within 3L Diamond. Each licence includes access to all supported devices and boards. Copious royalty-free examples and tutorials demonstrate the creation and simple movement of tasks around available hardware.

3L Ltd, www.3l.com

In-circuit programmer for ARM Cortex devices connects via Ethernet, USB or Serial Port

Computer Solutions has released an in-circuit programmer that supports ARM Cortex devices from Freescale, STMicroelectronics, Texas Instruments, and NXP. Once the Cyclone is configured, programming operations may be completed in one touch with or without a PC, says the manufacturer. The Cyclone and the target being programmed may be local to the PC or connected remotely via Ethernet. Multiple Cyclones on the network can easily be detected and controlled from the same PC. In addition, the Cyclone for ARM devices has been specifically designed with features like voltage protection technology in order to withstand the rigors of a production environment. In Stand-Alone Mode, the Cyclone for ARM devices is configured and loaded with one or more programming images. Control of the Cyclone may then be automated using a PC (e.g., for large production runs), or the Cyclone can be operated independently of the PC (e.g., for field updates). An LCD screen facilitates configuration and operation of the unit. The display's menu-based navigation allows the user to easily select the image to be programmed when the Cyclone for ARM devices contains multiple programming images. The unit works with the Freescale Kinetis (K, L), STM32, TI-(Stellaris - LM3S, LM4F), NXP (M0, M3, M4) ARM families. It supports 10 and 20 pin JTAG and SWD modes and works with 1.8V-5V targets. The unit also includes software for flash programming on chip memory of all supported CPUs and external Flash devices.

Computer Solutions www.computer-solutions.co.uk

Integrated development environment allows to record and display instruction trace data

Atollic's release of the TrueSTUDIO v4.1 integrated development environment incorporates many new features, including the ability to record and display instruction trace data. Other features include the addition of automatic software unit testing within the optional TrueVERIFIER add-on module, and a test case debugger within the optional TrueANALYZER add-on module.

The new instruction tracing function records the execution flow in real-time for later analysis. In this way, should an error occur it is possible to interrogate the trace logs and ascertain exactly what the processor was doing before a software error occurred. TrueSTUDIO v4.1 support ETM tracing using a Segger J-Trace JTAG probe, and ETB tracing for compatible ARM Cortex devices using any of the supported JTAG probes, such as the Segger J-Link. The recorded instruction trace log can be displayed in either C mode, mixed C and assembler mode, as well as in pure assembler mode. The trace log has graphical annotations on execution branches, and can be exported to a file for offline analysis. Integrating seamlessly with TrueSTUDIO, the optional TrueVERIFIER module now has an automatic software testing function that can check return codes and affected global variables for each function in the project. By examining your source code, TrueVERIFIER can automatically generate a test suite that is compiled, downloaded and executed on the target board automatically. On completion the test results and measured test quality data is transferred and visualized within the TrueSTUDIO IDE. The test engine and user Interface have also been updated within this new release. In addition, and ideally suit test driven development, TrueVERIFIER now also supports a test scenario mode, where more complex test scenarios can be designed.

Atollic www.atollic.com

Online simulation tool helps designers evaluate TI's InstaSPIN-FOC motor control

Texas Instruments has released a free, interactive online simulation tool that enables motor designers to assess the company's InstaSPIN-field-oriented-control (FOC) technology. This online simulation allows users to fully evaluate the software-sensor-based “sensorless” control for variable speed and load applications using three-phase, synchronous or asynchronous motors. Users can select from a library of motors, customize speed and load profiles and obtain simulation results within minutes. The simulation viewer enables users to view each waveform with a variety of zoom and pan options, perform numerous waveform analyses (e.g., period calculations, RMS, average) and print results. The entire experience is intended to give users confidence to proceed with motor designs using TI InstaSPIN-FOC motor technology. InstaSPIN-FOC removes the need for a mechanical motor rotor sensor, reduces system costs and improves operation using TI’s new software encoder (sensorless observer) algorithm, FAST (flux, angle, speed and torque), embedded in the read-only-memory (ROM) on TI's 32-bit C2000 Piccolo microcontrollers. The InstaSPIN-FOC online simulation tool is freely accessible.

Texas Instruments www.ti.com
100G Ethernet packet parser reference design kit using Tabula’s ABAX2P1 3PLD

Tabula now makes available a 100G Ethernet packet parser reference design kit based on its new ABAX2P1 3PLD and supported by its Stylus revision 2.6.2 compiler. The 100 GbE packet parser represents a novel approach to this class of network functions, delivering a unique combination of programmability and low latency. It provides support for multiple L2 accesses and trunk frame formats and is easily scalable to support L3 and L4 parsing. It also benefits from a very small footprint – less than 2K LUTs for a single 100G stream, making it an extremely cost-effective and power-efficient programmable solution that can be extended to support multiple 100G streams on a single chip. Tabula’s Spacetime architecture enables designers to co-optimize performance and density. Combining programmable fabric in which all components can operate at 2 GHz with multi-port high-performance memories. In this 100 GbE packet parser reference design, these capabilities are used to parallelize the processing of multiple fields of an entire 100 GbE packet header, enabling the parsing function to be completed in a record 17ns latency and making the parser software configurable to handle different L2 formats or extended to L3 and L4 parsing.

Tabula
www.tabula.com

Software version management system boosts distributed teams

Perforce Software has released version 2013.1 of its Software Version Management system, featuring enhancements to support globally distributed teams and scalable Agile development practices. The 2013.1 release focuses on two critical areas for software developers, codeline task management for greater workflow flexibility and advanced replication to support distributed teams. Advanced replication options in Perforce 2013.1 provide enhanced support, out of the box, for highly distributed teams to control exactly what is replicated in each location. Now every team gets high performance access to exactly what they need, when they need it. Perforce replication options are also tuned for high-performance build, test and release environments, enabling organizations to reach their goals for continuous delivery. Task Streams offer flexibility for managing tasks in progress. Task streams can also be archived upon completion of the task to de-clutter the stream graph. Along with task streams, shelving provides a flexible way to work on, review and promote shelved changes with quick approval. Shelves can be submitted directly or un-shelved to another branch. All Perforce products are provided free of charge for up to 20 users.

Perforce
www.perforce.com

Compiler qualification suite can be added into safety critical development tools

Dutch developer ACE Associated Compiler Experts has launched a compiler qualification suite for use in OEM software tool qualification kits and services. Safety standards like ISO 26262 require that adequate confidence and quality levels are demonstrated in software tools. C/C++ compilers translate software to hardware architectures and are complicated tools by nature thus requiring qualification and validation when used for safety critical applications. For this purpose, ACE has developed the SuperTest qualification suite which provides a unique level of compiler test coverage and can find hazardous problem cases in compilers. Using the new SuperTest qualification suite, system integrators and application developers using a tool chain can achieve the appropriate qualification and confidence levels for the compilers that are used when producing their applications. Developers of safety critical systems and applications can now have confidence in their compilers by testing these for their specific use cases using the SuperTest qualification suite. The SuperTest qualification product is available as an OEM product to be integrated into compiler specific qualification kits for tool vendors and through service companies.

ACE
www.ace.nl
Predictive modeling approach boosts the development of thin-film organic electronics

By Alexander Mityashin, David Beljonne, Jérôme Cornil, Claudio Zannoni, and Paul Heremans

IMEC (BELGIUM), University of Bologna (Italy) and University of Mons (Belgium) have developed a unique multi-scale methodology to model the development cycle for thin-film organic electronic materials and devices. This predictive approach has been applied in different case studies demonstrating its practical application. The new methodology will boost the development of organic electronics by providing a strong modeling help to experimental optimization.

The need for a new modeling methodology
Organic molecules have been exploited in a large variety of electronic and optoelectronic applications, such as organic light-emitting diodes (OLEDs), thin-film transistors (OTFTs), organic solar cells (OPV) and sensors. Several of these applications are currently making their first all-out attempts to enter the market. For many others, however, the technology is not yet there. Today, both the limited electrical performance and the environmental instability of molecular materials require major breakthroughs in their fundamental understanding. Among many strategies to facilitate the technology development, theoretical models are being sought to provide guidelines for material design and device architecture.

In this context, we have recently developed a new theoretical methodology for the predictive modeling of organic molecular semiconductors. Compared to existing instruments for molecular modeling, its conceptual novelty consists in integrating several state-of-the-art techniques into one multi-scale workflow. With the pivotal incentive of providing a comprehensive physical outlook, the proposed methodology covers various steps of the development cycle - from chemical design of new organic molecules to their thin-film assembly and electronic properties in devices.

Principle of the new modeling approach
The scheme of a typical modeling study is shown in figure 1 and includes three major steps. First of all, for every new molecular material that we would like to model, the physicochemical and electronic properties of individual molecules are parameterized by rigorous ab-initio modeling. These properties are essential to understand how these molecules interact together in solids, and how their interactions influence the thin-film morphology, its crystal structure and possible defects. Conjugating this understanding with molecular dynamics modeling, we construct molecular films of several thousands of molecules, with thickness up to a few tens of nanometers. These dimensions are appropriate for characterizing device-relevant electronic processes. In a similar way, one could model molecular deposition and thin-film growth processes, imitating the industrially-relevant fabrication techniques that we like to elucidate. Finally, electronic and electrical properties of the obtained films are revealed by combining micro-electrostatics and charge transport modeling. Micro-electrostatics is first applied to study the energy level landscapes for the charge transport. Later on, these landscapes are populated with mobile charges, identical to those injected from metal electrodes in thin-film devices. The motion of these charges is monitored by the charge transport modeling to reveal their speed and transport efficiencies; these properties are responsible for the material conductivity and charge carrier mobility.

To make this thorough integration possible, a certain technical innovation was required. Among many things, the most crucial one was to work out the communication protocols to enable individual methods to “talk” to each other. The smooth matching of characteristic scales, accuracies and computational complexities of different methods is assured by optimized and newly-developed data-exchange protocols. Once such framework is established, the work-flow of figure 1 is only an example of a possible modeling realization; many more techniques can be integrated as new modules, as illustrated in the figure by the stacks of candidate techniques available for every modeling block. Such integration results in a unique configurable platform for predictive modeling from nano-scale of individual molecules to macro-scale of thin-film devices.

Revealing the mechanism of molecular doping in organic semiconductors
The multi-scale methodology enables new strategies to tackle scientific challenges at scales and complexities that previously were not accessible by conventional modeling techniques or experiments. For example, we have applied this approach to unravel the mechanism of molecular doping in crystalline organic semiconductors. Monitoring the doping-associated electronic processes offered the first assessment of the doping mechanism at the molecular scale and of its efficiency.

The main steps of this study are summarized in the top part of figure 1. For the convenience of the experimental validation, we selected a well-known semiconductor-doping combination: p-type semiconductor pentacene and its complementary dopant F4TCNQ. After ab-initio parameterization of individual molecular properties of the host and doping materials, films
with different doping concentrations were constructed by introducing F4TCNQ molecules in the vacancies of the host crystal. To make this structure physically realistic, molecular mechanics was used to find the most likely orientation of doping molecules in the host crystal. Energetics for the doping-host charge donation and transport of these donated charges were modeled using micro-electrostatics and charge transport simulations. The ability to monitor these doping-associated electronic processes at the molecular scale provided several new insights into the efficiency of the doping mechanism and its sub-events. It allowed, for example, to complement the existing vision of charge donation with information about how the chemical and structural properties of doping and host molecules impact the charge donation efficiency. Even more importantly, the previously obscure process of free-charge generation has been clarified microscopically as a function of the doping concentration. These findings were compared to the experimental measurements showing excellent qualitative agreement.

The overall mechanism of molecular doping in organic semiconductors has been found to differ strongly from the conventional wisdom of inorganic materials. In organics, a strong correlation between the dopant efficiency and its concentration is demonstrated along with the threshold concentration of the doping activation. Strategies towards the design of more efficient doping involve a proper tuning of the host-dopant geometric and electronic interfaces.

Outlook to further applications
To give an outlook to further applications of the multi-scale methodology, it is important to notice that similar models can be used to investigate the influence of impurities or effects of environmental degradation of organic materials, for example due to oxygen or water penetration into organic films. Generally speaking, one can envisage many more applications of our methodology for in silico optimization of hetero-interfaces in organic optoelectronic devices or, alternatively, for de novo molecular design of interfaces with tailored properties.

For example, we are currently studying how charge generation in organic solar cells depends on the material selection and nano-architecture of their donor-acceptor interfaces; we perform similar modeling for dielectric-semiconductor interfaces in organic thin-film transistors. We also foresee multiple avenues for the further development of the multi-scale toolbox of methods. A natural leap in development will be done towards easier integration of new materials. Comparing different materials is the primary practical duty of the developed methodology. An easy, modeling-friendly procedure is therefore required to automate the integration of new molecules into simulations. Given the skyrocketing progress in the chemical engineering of new organic molecules, rapid material succession is likely to be the case, and will probably even accelerate in the future. Therefore, modeling tools must be capable of quick and reliable integration and testing of new (maybe even not-yet-existing) materials.

We anticipate that this new approach to modeling will assist the progress of experimental and theoretical work on the aforementioned problems, and many more of those we have not (yet) conceived of. We established evidence that this methodology provides a computationally efficient framework to link the molecular properties of the constituent material to the resultant electronic device performance. This should fuel further studies of electronic processes in the heart of OTFT, OPV and OLED device operation, with the long-term goal of becoming an instrument to facilitate the development of materials and devices. Multi-scale modeling can inform the rational design of optimized molecular materials for organic electronics, eventually advancing better performance and more durable materials. Application in device building may also lead to improved electrical performance and perhaps even to novel device concepts and architectures. It will ultimately facilitate the experimental validation cycles that are needed to improve on existing organic electronic materials and devices.

Fig. 1: A typical modeling study includes three major steps: looking at the molecular material level, experimenting with device fabrication and assessing device operation.
A new class of flexible semiconductors enters the market

By Mike Cowin

RECENT REPORTS by HSBC Global Research and by IHS predicting global shipments of flexible displays to hit 800M units by 2020 coupled with recent announcements that LG plans to launch a flexible OLED product by Q4 2013 show the flexible display market is at a tipping point and 2014 is set to be an important year for the industry.

It is clear that significant technology gaps existed in the evolving supply chain for flexible semiconductors in both inorganics and organic material offerings. Inorganic semiconductor materials pose serious concerns for manufacturers with the need for vacuum processes, high-temperature procedures - a key barrier for use with flexible plastic backplanes and most significantly unproven flexibility in final form. Historic concerns regarding organic semiconductor were low carrier mobility, temperature resistance and controllable uniformity in TFT (Thin-Film-Transistor) performance.

Nevertheless the compelling benefits over inorganics offered by organics such as inherent flexibility and the potential for solution processing with a wide range of substrates, print processes and device architectures meant that if these prior art issues could be resolved a real enabling product would exist for the flexible market.

To meet these requirements SmartKem’s approach was to develop a new class of semiconductors called p-FLEX. These semiconductors use high mobility small molecule materials with proprietary binder matrix materials to yield exceptionally high performance solution-based semiconductors that can be processed in air, offer highly uniform films, are stable up to and above 250°C and are fully compatible with a range of print processes.

The development of organic semiconductors (OSCs) generally falls into two main categories of materials: polymeric and distinct molecular materials. A common feature is that both these types of materials are conjugated systems, that is to say they consist of alternating single and double bonds. Key consideration also has to be given to matching the highest electron energy level of the OSC to the work function of a metal contact to ensure efficient device operation.

For high performance TFTs, high charge carrier mobility is required and this favours crystalline small molecule semiconductors. While close packed and regular arrangement of the molecule crystal lattice give rise to good n-overlap and efficient charge carrier mobility these materials on their own tend to demonstrate anisotropy.

This new class of semiconductor materials eliminates such issues by designing into the inks the preferred features of chemically stable, high mobility, single-crystal organic semiconductors and combining this with amorphous semiconducting polymers and the uniform processing characteristics that these binders offer.

When looking at prior art, solution printing of semiconductors has tended towards either solution printing of single-crystal films or printing small molecule semiconductors in polymer blends. Printing single-crystal organic semiconductors such as substituted benzothienobenzothiophenes in solvents has managed to yield impressive carrier mobility’s of up to 30 cm²V⁻¹s⁻¹, but with the serious disadvantage of the yielding very poor device to device uniformity and mobility values ranging between 1 to 32 cm²V⁻¹s⁻¹ - great in the lab and for headline results but not practical for real world applications. Whereas the printed small molecule-polymer blend approach afford good device uniformities that are becoming industrially interesting, but with very low mobility’s of only around 1 cm²V⁻¹s⁻¹ and an inability to control the performance of the formulated blend in top gate and bottom gate TFTs.

SmartKem’s semiconductor approach overcomes these technology roadblocks by carefully engineering chemical improvements into its material molecular framework. These inks incorporate polycrystalline small molecules that have been designed with the highest levels of pi-pi overlap and minimum inter-planar pi-pi distances when deposited with the optimum crystal packing in the printed semiconductor layer. The key to achieving this effect in printed layers is to use the small molecule in combination with a new class of patented “matched”

Fig. 1: Typical morphology of the SmartKem p-Flex.

Fig. 2: SmartKem’s formulation facility at Technium OpTIC in St Asaph, UK.

Mike Cowin is Head of Product Development at SmartKem - www.smartkem.com
of semiconductor inks now consist of a range of high mobility polycrystalline small molecules in combination with seven distinct chemical classes of customised semiconducting polymers, these are the subject of a series of unpublished patent applications.

When it comes to performance, these inks have been rigorously tested both internally and externally at centres of excellence such as CPI in the UK and by industrial partners (and offers for TGBT TFT’s) charge mobility in excess of 5 cm²V⁻¹s⁻¹, threshold voltages near zero and on-off ratios of the order of 10⁵ for un-isolated devices. These solution-based semiconductors thus outperform a-Si and are comparable to most oxides, but with the key advantage of inherent flexibility and ambient temperature processing - a "must have" for most flexible plastic substrates. In addition, initial pilot line trials are exhibiting excellent levels of TFT uniformity due to ability to control film formation at a molecular level.

Table 1: Comparing potential semiconductors for flexible displays.

<table>
<thead>
<tr>
<th>Technology Type</th>
<th>Intrinsic properties</th>
<th>Ease of Manufacture</th>
<th>Customisation Potential</th>
<th>Device Performance Potential</th>
<th>Cost-down Potential via printing</th>
</tr>
</thead>
<tbody>
<tr>
<td>p-FLEX</td>
<td>Good</td>
<td>Excellent</td>
<td>Excellent</td>
<td>Excellent and Stable</td>
<td>Very High</td>
</tr>
<tr>
<td>a-Si</td>
<td>Limited</td>
<td>Good for LCD only</td>
<td>Very Limited</td>
<td>Not Flexible</td>
<td>Limited</td>
</tr>
<tr>
<td>LTPS</td>
<td>Excellent</td>
<td>Poor for Flex Electronics</td>
<td>Very Limited</td>
<td>Not Flexible</td>
<td>Very Limited</td>
</tr>
<tr>
<td>IGZO Sputtered</td>
<td>Very Good</td>
<td>Poor for Flex Electronics</td>
<td>Very Limited</td>
<td>Not Flexible</td>
<td>Very Limited</td>
</tr>
<tr>
<td>IGZO Solution</td>
<td>Limited</td>
<td>Poor for Flex Electronics</td>
<td>Limited</td>
<td>Not Flexible</td>
<td>Very Limited</td>
</tr>
<tr>
<td>N-Type Si Printed</td>
<td>Excellent</td>
<td>Poor for Flex Electronics</td>
<td>Limited</td>
<td>Not Flexible</td>
<td>Very Limited</td>
</tr>
</tbody>
</table>

The electrical and physical specifications of this new range of semiconductors already meet the requirements for both EPD and OLED and can be processed on a wide range of material surfaces, such as glass or plastic using print processes such as ink jet, slot die or roll-to-roll. Critically this offers the end user the potential to make the transition to continuous print techniques and reduced cost of production as these systems come online.

In the short term, new curved form factor products in the next six to twelve months will most likely incorporate low mobility, high temperature inorganics on glass via a legacy of traditional kit and materials. However whilst inorganics are a quick fix to the very immediate need for new product, the medium to long term needs of the flexible display industry will inevitably move towards low temperature, solution-based organics where the material performance and process advantages are just too compelling to ignore. For instance an organic front plane coupled with an organic back plane makes sense, especially when you throw into the mix the potential for continuous roll to roll production.
Printed electronics opens up large flexible sensor design opportunities

By Laurent Jamet

**COMPARED TO TRADITIONAL** electronic solutions, printed electronics offers several differentiating factors which make them particularly well suited to sensing application. Most printing processes are compatible with large area substrates, which enable the design of large area sensors with sensing capabilities across surfaces of up to 500x500mm. This at a very competitive cost per area ratio (compared to amorphous silicon or CMOS technologies).

A pioneer in printed electronics applied to optical sensors, Isorg addresses several markets and functionalities. This includes scanning surfaces for X-ray digital imaging with the co-integration of organic photodiodes with transistors on amorphous silicon, fully integrated in printed electronics with organic photodiodes combined with organic transistors on plastic substrate.

In the future, substituting amorphous silicon technology with organic electronics will increase cost competitiveness and enable new products developments (for lighter and more robust portable equipment). The first demonstrator of such a full organic image sensor is being fabricated as a collaborative development between Isorg and Plastic Logic. More particularly, the collaboration focuses on the deposition of organic printed photodetectors onto a plastic organic thin-film transistor backplane, to create a flexible sensor with a 40x40mm active area, 375um pitch (175um pixel size with 200um spacing) and a 94x95 = 8 930 pixel resolution – see figure 1.

Biometrics applications using fingerprint and palmar surface recognition could use printed electronics to substitute the typical CMOS-based sensors with thinner and lighter organic solutions. Current developments yield a pixel resolution of 50um. Such approaches could also enable the design of large scanning surfaces to substitute CCD line scanners in office equipment, yielding faster, lighter and thinner document scanners. So far in this field, a pixel resolution of 80um has been achieved for a 300 dpi document scanning resolution.

Printed electronics also finds its way in temperature sensors in printed electronics (figure 2), applying its large area sensing capabilities to the detection of hot spots, for example to monitor the power distribution and heat dissipation in power electronics circuit boards.

**Thin and flexible: a system-on-foil approach**

Using PET as a substrate, it is now possible to design system-on-foil sensing solutions that combine optical sensors, discrete components such LED and flexible interconnections. In this way, contactless user interfaces can be built using organic photodetectors, offering functionalities such as hand proximity detection and gesture recognition for power on/off or linear control (slider and vertical distance detection). These conformable system-on-foil user interfaces can even be integrated in smart textiles products. The optical solution relies on the detection by organic photodetectors of the reflected infra-red light emitted by IR-LEDs directly mounted on a flex circuit, as shown in figure 3. For this purpose, the organic semiconductor materials can be tuned to operate both in visible and near infra-red bands. Being very thin and easy to glue to other substrates such as paper, these new sensors can easily turn plastic and paper...
Large-area fully-organic flexible photodetector array ready for x-ray imaging

At this year’s International Image Sensor Workshop, imec and Holst Centre presented a large-area fully-organic photodetector array fabricated on a flexible substrate. The imager is sensitive in the wavelength range suitable for x-ray imaging applications.

Because of their very high absorption coefficient, organic semiconductors allow extremely thin active layers (10 to 50nm). Also, given their low processing temperature, they can be processed on foils. As a result, organic imagers can be more robust and light-weight compared to their traditional counterparts and may be used for conformal coating of randomly shaped substrates. Moreover, the wide variety of organic molecules available ensures that the properties of the active layer can be tuned to applications requiring specific wavelength ranges.

The presented imager is sensitive in the wavelength range between 500 and 600nm, making it compatible with typical scintillators and therefore suitable for x-ray imaging applications. It was fabricated by thermally evaporating an ultrathin (submicron) photosensitive layer of small organic molecules (SubPc/C60) on top of an organic readout circuit.

A semi-transparent top contact enables front-side illumination. The readout backplane was manufactured on six inch foil-laminated wafers. It consists of pentacene-based thin-film transistors (TFTs) in arrays of 32x32 pixels with varying pitch (1 mm and 200 µm). To prevent degradation of the organic semiconductors in the air, the photodetector array is encapsulated.

The imager was characterized under illumination with a calibrated green light-emitting diode (LED), yielding a linearly increasing photocurrent from the incident power of 3 µW/cm². Dark current density is below 10-6 A/cm² at a bias voltage of -2V.
Fully instrumented sock integrates smart fabrics sensors to provide fitness data

Washington-based startup company Heapsylon has launched an USD87,000 crowdfunding campaign on Indiegogo to finalize product development and manufacturing of its Sensoria Fitness system. This includes smart socks with smart fabrics sensors, an electronic anklet for communicating the data with the user’s mobile phone, and a virtual coach mobile app. The sock shaped Sensoria device is able to track everything from foot landing and stride cadence to activity level and altitude gain. The specially chemically-treated fabric Sensors are able to measure pressure points for a detailed analysis of the foot’s contact with the sole. With these socks on, every time you walk, run and exercise you are generating valuable data that can be processed to produce meaningful views of your activity and the way you use your whole body (in this instance, the way you articulate your feet onto the ground). The sensor filled sock is comfortable, washable and designed for runners. The smart fabrics Sensors send pressure data to the Sensoria Anklet. The Sensoria Anklet uploads data wirelessly either via computer or through a smartphone. The data is then added to a dashboard for either retrospective analysis or instant coaching. After over two years of research and development the Heapsylon Sensoria wearable devices are now at prototype stage, with appropriate funding, the devices could be commercialized in 2014 for about $150.

Touch screen technology goes behind the display

Peratech has used its recently launched QTC Ultra sensor to create a touch screen solution for OLED displays for phones, monitors and large interactive displays. The QTC Ultra sensor is so sensitive that it can be placed behind the OLED display and still detect finger touches on the front of the display to create a touch screen interface. By positioning the touch screen sensor behind the display, there is no loss of light from the display enabling the battery life to be longer. Currently, Sensors go over the display and absorb light which has to be compensated for with a brighter setting for the display and that uses up more battery life. The QTC Ultra sensor works best with OLED and e-paper type displays, which are becoming increasingly popular, although it can be used with other display technologies providing they can be pressed. The Sensors rely on Peratech’s Quantum Tunnelling Composite (QTC) anisotropic material which changes its resistance at the point where pressure is applied. A deflection of a micron or so is needed for QTC Ultra to sense the touch through the layers of glass and display. The solution provides not only multi-touch x and y co-ordinates but also z according to the amount of pressure applied enabling new gesture inputs to be created. The layer of QTC material is printed as a QTC ink on the back of the display as required by the product designer.

Translucent flexible antenna film is only 130 to 185 microns thin

Pulse Electronics’ mLUX Translucent Flex antenna is an invisible antenna concept that allows light and colour to shine through the translucent device cover, offering multiple options for industrial design. When integrated into the display, the antenna enables increased use of metal on the back cover of the handset. The mLUX flex antenna provides state-of-the-art RF performance and can be placed as far away as possible from the ground plane and the user’s hand, improving performance significantly. The device thickness can be reduced while achieving the same performance as standard flex antenna solutions. The antenna can be assembled to the display, covers, or a separate carrier with adhesive or, alternatively, it can be moulded between clear and opaque plastics. When the antenna is placed near the display, smaller feeding elements can be used, reducing the total volume needed for the antenna. Total thickness of the flex is 130-185µm with a copper (Cu) thickness of 12µm. Non-pattern areas are filled with mesh to achieve a surface that is equally reflective throughout. The Cu mesh line-width is 12-20µm with 300µm pitch and the flex transmittance is typically around 80%. These RoHS compliant antennas are customized for each application and design and are available and ready for volume manufacture.

Heapsylon
www.heapsylon.com

Peratech
www.peratech.com

Pulse Electronics
www.pulseelectronics.com
Efficient geolocation using swarm radio

By Gunter Fischer, Thomas Förste and Frank Schlichting

IN WIRELESS SENSOR networks the concept of a swarm is used to illustrate how individuals in a group interact. Individuals in a swarm need to know their position relative to each other. Nanotron has added location-awareness to wireless sensor networks so that the swarm members can measure the distance between each others, and are able to make decisions using this information. Communication and location awareness together are enabling a whole new category of geolocation applications.

Collision avoidance (CAS) - to mention just one of them – is introduced in this article to illustrate the benefits of an extended swarm approach.

The swarm platform technology

Low power swarm radios – autonomous 2.4 GHz Chirp Spread Spectrum wireless nodes – are the basic swarm building blocks – see figure 1. They are able to broadcast and exchange messages while monitoring distances to other individuals in the swarm which are the key capabilities that allow for coordinated swarm behavior.

![Figure 1: The swarm radio mini from nanotron.](image)

Each individual in a wireless swarm consists of a swarm radio that is controlled by a host through its application interface (API). There are several categories of API commands – see figure 2.

- The **RangeTo** <node ID> command for instance returns the distance to another node.
- The quality of location-awareness depends on two basic criteria: accuracy and latency. Accuracy is the difference between measured and true distance. Usually it could be characterized by a fixed offset and the spread of results as shown in figure 3. Latency specifies the time required to obtain a ranging result. It has a strong impact on the real-time character of the application. Short messages and quick responses help to minimize latency thus maximizing throughput. A typical swarm radio requires 1.8 milliseconds of air time for executing a SDS-Twr cycle, nanotron’s patented Symmetrical Double-Sided Two Way Ranging. To broadcast its ID it only requires 350 microseconds.

The maximum obtainable range of the swarm radios determines how far apart individuals in the swarm are still able to interact. Maximum range is highly dependent on the application environment.

Under ideal line-of-sight conditions range might exceed 500 meters; however, in reality it will often be much shorter due to obstacles, reflections, interference from other radio signals, antenna miss-alignment etc.

Figure 4 shows a real world example with one swarm radio inside a car and the other carried by a person. Range could be extended by placing the antenna on the outside of a car or by having the antenna installed on a hard-hat instead of on a belt.

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Dr. Frank Schlichting is Director of Product Management for the swarm product line at nanotron. He can be reached at f.schlichting@nanotron.com.

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**Fig. 1:** The swarm radio mini from nanotron.

**Fig. 2:** Overview of nanotron’s swarm API commands.
Collision avoidance solution (CAS)

There is a need for automatic collision avoidance in mining. In order to prevent accidents a reliable alarm is required whenever vehicles come too close to people, assets or other vehicles. The swarm geolocation technology is well-suited for implementing such collision avoidance solutions (CAS).

A simplified set-up with vehicles, assets and people – a total of three node types – is used to illustrate the essential outline of the application. In the worst case scenario two objects move towards each other at maximum speed – see table 1. The system needs to react faster than the time necessary for the objects to traverse the respective safety zone for the shortest path collision course. In our example the shortest time is 2.2 seconds; therefore latency of the CAS system must be kept short and the whole group of nodes needs to complete the full location awareness cycle faster than in 2.2 seconds. For reliable operation one might decide to accelerate the sequence in order to execute it several times within this interval.

Figure 5 shows the steps of the location awareness cycle and how they are supported by the swarm radio:

- Get IDs (4): As a first step the swarm radio makes itself visible by broadcasting its own ID. SetBroadcastInterval=01 for example sets the blink interval to 1 second. After activating the broadcast by SetBroadcastNodeID=1 the swarm radio broadcasts its ID every second. Node IDs of other participants are automatically stored in the NodeID list when received. The host application can read the NodeID list by using the GetNodeIDList command. This way neighbors are identified to the CAS application.

- Range to IDs (5): As a second step the swarm radio measures the distance to all neighbors. This is accomplished by subsequently executing the RangeTo <node ID> command. Resulting distance values are communicated back to the host application.

- Evaluate distances (6): In a third step the CAS application needs to decide whether any of the measured distances violates a safety zone requirement and needs to take action if it does. It may involve a simple audio alarm on approach or exercising the brakes of a truck to prevent an imminent collision.

As part of designing the CAS application it is now possible to estimate the time required to execute one location awareness cycle and trigger an alarm if required. The sequence in our example takes less than 30 milliseconds; hence the time constraint mentioned above can be easily met.

All swarm radios share the same air interface. The CAS application works in an entirely asynchronous fashion and packet collisions may occur. Several location awareness cycles instead of just one increase the probability of a successful sequence. At the same time traffic through the air interface must not exceed channel capacity. Broadcasting the node ID together with a full ranging cycle takes about 2.2 milliseconds of the air time. This is just 0.1% of the 2.2 second cycle time for the CAS application. As a rule of thumb no more than 17% of the available airtime should be used as a good trade-off between success rate and throughput. This is important when scaling the application by adding more swarm radios.

In real swarm applications safety zones could be designed to be dynamically adjusted to the actual speed of the moving object and the last measured distance on a potential collision course. This way the total number of alarms can be minimized and the number of swarm radios that can be used in the system before channel saturation occurs, can be maximized.

Nanotron’s swarm platform is well-suited to build geolocation applications quickly. Swarm radios are location aware since they are able to measure distances amongst themselves and exchange the results. Range, ranging accuracy, latency and throughput are important design criteria for geolocation applications based on the swarm platform.
Global navigation satellite system engine supports fully concurrent GLONASS, GPS, QZSS and SBAS

CSR has debuted the SiRFstarV 5e, a Global Navigation Satellite System (GNSS) engine optimised to enable highly accurate location positioning for devices including mobile phones, cameras, and health and fitness products. By supporting fully concurrent GLONASS, GPS, QZSS and SBAS from ROM, the highest accuracy and fastest time-to-first-fix (TTFF) are ensured. Wireless solutions specialist Teilt Communications plc will be using the device for its Jupiter SE868-V2 module, which was launched at CTIA Wireless 2013 in Las Vegas. The 11x11mm QFN packaged receiver module integrates 5e, TCXO, SAW and RTC oscillator into a small convenient package, accelerating time-to-market and reducing product development risks. SiRFstarV 5e offers a range of features to increase accuracy, improve time to first fix and preserve battery power to enable a better user experience. These include InstantFix Extended Ephemeris (EE) with autonomously forward predicting EE for three days locally. The GNSS chip can connect directly to a Lithium battery supply, enabling system cost reduction and increased power efficiency.

CSR
www.csr.com

Telematics test platform addresses in-vehicle testing

With cars increasingly incorporating telematics functions and features, testing of telematics devices becomes an issue for OEMs and tier ones. RF testing expert company IZT GmbH has developed IZT RecPlay, a platform for RF receiver design validation of analog and digital radio, video and global navigation satellite systems. The platform features a portable monitoring RF recorder for mobile and telematics applications for accurate phase-synchronous recording of diversity signals from multiple antennas. Customers benefit from the lightweight Recorder with a 30-cm high-resolution touch screen as a turnkey solution for in-vehicle testing. The integrated GPS receiver serves as a highly robust time and location reference. RecPlay's signal generator IZT S1000 combines 31 virtual signal generators in a single platform for testing radio receiver and for creating complex mixed signal RF scenarios. The system receives, records, and replays up to 20 MHz bandwidth in a frequency range from 9 kHz to 3000 MHz. It supports practically all radio broadcast standards.

IZT
www.izt-labs.de/en/home/

GPS tracking module takes less than 29s for cold-start time to first fix

SkyTraq Technology’s next generation Venus 8 platform supports GPS, GLONASS, Beidou2, Galileo, QZSS, and SBAS, doubling the search engine capability and reducing more than half the power consumption from its previous generation. The Venus 8 integrates high performance GNSS signal-processing engine, low-power 32-bit RISC, IEEE-754 compliant FPU, cache memory, real-time clock, backup RAM, LDO regulator, switching regulator, GPIO, UART, SPI, I2C, ADC and all the necessary program ROM and data RAM on-chip for direct PVT solution with NMEA output in stand-alone GNSS applications. Using high-performance search engine and track engine architecture, the Venus 8 is capable of acquiring and tracking 167 satellites simultaneously, achieving fastest signal acquisition and TTFF in the industry, according to the manufacturer. It achieves cold-start TTFF of less than 29 seconds and hot-start time of 1 second. Having -165dBm tracking and -160dBm reacquisition sensitivity, the module allows continuous navigation in nearly all environments. It draws 6mA under continuous navigation and comes in a 5x5mm QFN40 package.

SkyTraq Technology
www.skytraq.com.tw

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SkyTraq Technology
www.skytraq.com.tw
Freescale both low-end and high-end Radar modules.

To achieve a total system solution for radar-based ADAS solutions with other safety-oriented advanced driver assistance systems (ADAS), Radar is one of the central sensor technologies. Chipmaker Freescale now has introduced a comprehensive system-level solution for automotive Radar based advanced driver assistance systems. The new Qorivva MPC577xK Microcontroller (MCU) and MRD2001 77 GHz Radar transceiver chipset provide the embedded technology necessary for affordable Radar based ADAS solutions with fewer components, helping increase the adoption of such features in mainstream vehicles. The Qorivva MPC577xK MCU, built on Power Architecture technology, provides high-level digital and analog integration in a single-chip solution for Radar applications, removing up to four additional major printed circuit board (PCB) components and reducing system-level cost, PCB space and software complexity. The MCU also provides high performance for intense computational tasks with key integrated digital accelerators and features a state-of-the-art signal processing toolbox that contains all of the hardware modules required for processing sampled signals from short-, medium- and long-range Radar applications. Performance data from the European New Car Assessment Programme (Euro NCAP) suggests that safety systems, such as Autonomous Emergency Braking (AEB), can reduce accidents by up to 27% and can lead to a considerable reduction in road injuries. Euro NCAP plans to incorporate the AEB assessment for cars sold in Europe into its five star rating scheme beginning 2014.

Using Freescale’s new Radar transceiver chipset, automakers can implement long-range and mid-range frontal Radar for adaptive cruise control and autonomous emergency braking systems, as well as manage blind spot and side-impact detection – all through a single, scalable, multi-channel solution. Designers can pair the Radar transceiver chipset with the Qorivva MCU to achieve a total system solution for both low-end and high-end Radar modules.

Freescale
www.freescale.com

Battery-free switch tag tracks open/close status

Wireless, battery-less Sensors can now be embedded in products to track open/close status with the new X1GLADIO passive switch from Farsens S.L. The battery free RFID switch is compatible with commercial EPC C1G2 readers and communicates a unique ID and the associated switch status data without the need of battery supply on the sensor tags. The tag comes in a variety of antenna designs and sizes to adapt its performance to the required application. The reading distance for the battery-free pressure-sensor tag is around 2.5m and it can be embedded in a wide variety of materials such as plastics or concrete. The device features one of three different Connectors for users to connect their switch: a 2.00mm pitch SIL latched vertical pin header, a 2.00mm pitch male 1x2 header or just the 1x2 header footprint (pitch 2.00mm). The X1GLADIO is suitable for use in applications where monitoring of open/closed or connected/disconnected components is needed.

Farsens S.L.
www.farsens.com

50mm diameter ring type encoder for dial-type controls

In the automated driving scenarios of the future and in many other safety-oriented advanced driver assistance systems (ADAS), Radar is one of the central sensor technologies. Chipmaker Freescale now has introduced a comprehensive system-level solution for automotive Radar based advanced driver assistance systems. The new Qorivva MPC577xK Microcontroller (MCU) and MRD2001 77 GHz Radar transceiver chipset provide the embedded technology necessary for affordable Radar based ADAS solutions with fewer components, helping increase the adoption of such features in mainstream vehicles. The Qorivva MPC577xK MCU, built on Power Architecture technology, provides high-level digital and analog integration in a single-chip solution for Radar applications, removing up to four additional major printed circuit board (PCB) components and reducing system-level cost, PCB space and software complexity. The MCU also provides high performance for intense computational tasks with key integrated digital accelerators and features a state-of-the-art signal processing toolbox that contains all of the hardware modules required for processing sampled signals from short-, medium- and long-range Radar applications. Performance data from the European New Car Assessment Programme (Euro NCAP) suggests that safety systems, such as Autonomous Emergency Braking (AEB), can reduce accidents by up to 27% and can lead to a considerable reduction in road injuries. Euro NCAP plans to incorporate the AEB assessment for cars sold in Europe into its five star rating scheme beginning 2014.

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Freescale
www.freescale.com

50mm diameter ring type encoder for dial-type controls

Alps Electric Europe has developed the “EC50A Series” ring type encoder for use in controls for car air conditioning and audio systems or major home appliances. Dial-type devices have often been used in the past for car air conditioning and audio system controls. These devices are often designed to enable embedding of a control switch or a small LCD in the center of the dial. But design freedom cannot be enhanced without widening the device’s inside diameter (central opening). Space around the control panel is limited, hence, opening up the inner diameter is one way to make some room for an extra switch, LEDs or a small LCD, while retaining the same external dimensions. The EC50A Series is claimed to be the industry’s first 50mm ring type encoder, with a large 37mm inside diameter that provides a central opening around twice as large as Alps’ earlier product. The EC50A Series also has a guide formed on the inner wall to reduce rattle when the customer attaches a knob. Furthermore, original mechanical design and precision processing technologies were applied to achieve a premium operating feel.

ALPS Electric
www.alps.com

350mW GaN on silicon LEDs operate from 350mA to 2A in pulse applications

Plessey has announced that samples of samples of its PLB010350 350-mW LED products are now available. The entry-level lighting devices are manufactured on Plessey’s 6-inch MAGIC (Manufactured on GaN I/C) line at its Plymouth, England facility. The new LED products are aimed at a variety of solid state lighting and entertainment-type lighting products including accent lighting, wall washing, wall grazing, strip-lighting and a variety of pulse lighting applications. Barry Dennington, Plessey’s COO, said: “The MAGIC LED product range is expanding in both light output and efficacy. The PLB010350 is our first, high current device operating at anywhere from 350 mA through to 2 A in pulse applications. We have also been able to demonstrate the versatility and the potential of the Plessey GaN on Si technology by constructing an LED with a relatively large die area. This new 350 mW product demonstrates the inherent flexibility we have for the manufacture of LEDs with a 6-inch GaN on silicon substrate in an integrated circuit manufacturing line. We are seeing continual improvements in output efficiencies in the lab which means we will continue to launch new products in line with our product release plan.” The use of Plessey’s MAGIC GaN line using standard semiconductor manufacturing processing provides yield entitlements of greater than 95% and fast processing times providing a cost advantage compared with standard LEDs of similar quality.

Plessey
www.plesseysemiconductors.com
Smart-meter SoC supports Meters-and-More open communication standard

STMicroelectronics has announced a smart-meter IC with built-in support for the Meters-and-More open communication standard, which enables widespread interoperability among smart metering equipment using Power Line Communication (PLC). The ST75MM is claimed to be the first to embed hardware and communication protocol support for Meters-and-More, simplifying meter design to ultimately enable faster, lower-cost and reliable deployments. The IC enables designers to benefit from the protocol’s strong features for smart meter and advanced metering infrastructure applications, such as short messages, robust encryption and authentication features, support for network configuration and management, and retransmission management. First samples of the ST75MM, in the 7x7mm QFN 48 package, will be available to selected customers by October 2013.

STMicroelectronics
www.st.com

PCB terminations enable flexible power distribution in lighting and control systems

Harting’s new Han-Fast Lock PCB termination system provides simple solder-free push-fit single-wire connection to printed-circuit boards, greatly enhancing the ease and flexibility of power distribution for entertainment equipment such as lighting dimmers, Power Supplies and winch/hoist motor controllers. Power-line terminations can now be taken from any point on the printed-circuit board without the need for tracks to be extended to one specific connection area. As a result, costs are reduced because of the simplified design and savings in real estate. This approach also eliminates the possibility of concentrated “hot spots” and therefore allows higher currents to be handled. The easy “push/click” Han-Fast Lock PCB termination fits securely in the standard plated-through hole with pad and can handle up to 60 A for discrete wire stranded conductors from 4 to 10 mm². Undamaged contacts can be extracted and re-fitted up to ten times, simplifying equipment maintenance. In addition, during the production assembly process the connection for the external power wiring can be done after the soldering of the sensitive electronic components.

www.harting.com

Long-range RFIC platform has a range of up to 15km for M2M deployments

With a range of up to 15km, the SX1272 RFIC from Semtech enables metering, control and sensor applications. This device integrates Semtech’s new LoRa (long range) modulation technology to enable drastic range improvements over alternative modulation methods. In comparison, the maximum distance today of a smart meter transceiver in Europe using FSK modulation is between one and two kilometers. The additional range provided by LoRa will eliminate the need for repeaters in these applications, significantly simplifying the system design and lowering the total cost of deployment. The range extension provided by LoRa also makes the device suitable for emerging smart city, Internet of things (IoT) and machine-to-machine (M2M) applications. The SX1272 achieves receiver sensitivity up to -137 dBm using a low-cost crystal. This compares to today’s state-of-the-art FSK devices that can achieve sensitivity of -115 dBm with a comparable crystal or -125 using an expensive temperature controlled crystal oscillator (TCXO). Additionally, the SX1272 has a 25 dB improvement over FSK devices for rejecting in-band interfering signals. The SX1272 supports GFSK, FSK, GMSK, and OOK modulation in addition to LoRa and is designed to support WMBus, IEEE 802.15.4g (SUN), FCC 15.247, ARIB 796/108, EN 300-220 as well as other worldwide standards and regulations. Operating from a 1.8 to 3.7V supply range, the SX1272 draws 9.7 or 10.8mA for the receiver, 28mA for the transceiver at +13dBm, and has a sleep current of 100nA. It supports bit rates up to 300 kbps.

Semtech
www.semtech.com

125°C, ROHS compliant multilayered polymer capacitors

Cornell Dubilier’s Type CS multilayered polymer capacitors are designed for 125 °C applications with 6/6 ROHS compliance. Terminated with multiple pin connections, Type CS capacitors have low equivalent series resistance making them an excellent choice for switching power supplies, DC to DC Converters and other high ripple current applications. Available in capacitance values ranging from 2.0 µF to 10.0 µF, voltage ratings of 50, 100, 250, 400 and 500 Vdc, and current ratings up to 18A rms, Type CS capacitors cover a broad range of applications in power electronics where high capacitance and high current are needed for DC filtering. Type CS capacitors have multiple pin leads, up to 18 on the larger sizes, and UL94V-O rated epoxy exterior with the ability to pass 85 °C/ 85% RH requirements for demanding applications in military vehicles and aerospace.

Cornell Dubilier
www.cde.com
Optical jack sockets offer immunity to signal noise

Cliff Electronics’ optical jacks are virtually unaffected by electrical noise when transmitting and receiving digital signals. Seven different models are available that conform to the EIAJ/JEITA F05 standards for digital audio interfaces including fibre-optic interconnections. Matching moulded optical lead assemblies are also available for use with all them. The optical jacks operate with a supply voltage of -0.5 to 7.0V maximum, they take an input voltage of -0.5 to +0.5V maximum and operate in the -20 to +70°C temperature range. Insertion force is 5.9N minimum to 39.2N maximum, withdrawal force is 5.9N minimum to 39.3N maximum. Body material is PBT +30G, ABS 94-V-O (depending on model) with the shutter made from nylon PA66. The optical jacks are available as single or dual optical transmitter/receiver versions with the shutter made from nylon PA66. The optical jacks are available depending on individual connector type.

Cliff Electronics
www.cliffuk.co.uk

Transmissive optical sensors target encoder applications

Vishay Intertechnology introduced two new AEC-Q101-qualified surface-mount transmissive optical Sensors for automotive and industrial applications. Designed for harsh low- and high-temperature environments, the single-channel TCPT1350X01 and dual-channel TCUT1350X01 feature a wide operating temperature range of -40 °C to +125 °C. The TCPT1350X01 and TCUT1350X01 can be used as position Sensors for encoders in high-temperature environments close to motors, in addition to ignition locks and adaptive headlights. Both sensors can detect motion and speed. With dual channels, the TCUT1350X01 can also be used to detect direction in applications such as electronic power steering (EPS) systems. The single-channel TCPT1350X01 includes an infrared emitter and phototransistor detector located face-to-face in a surface-mount package while the dual-channel TCUT1350X01 includes an infrared emitter and two phototransistor detectors. Both sensors have a phototransistor output and an aperture of 0.3 mm, and each operates at a wavelength of 950 nm. The sensors feature compact dimensions of 5.5x4x4mm and offer typical output current of 1.6mA. With a 3.0 mm gap width, the devices can be used with a wide variety of materials and allow for looser mechanical tolerances than sensors with smaller gaps, making them suitable for automotive and industrial applications.

Vishay Intertechnology
www.vishay.com

LED driver features internal PWM generator to offer dimmer benefits

The LT3955 is a DC/DC converter designed to operate as a constant-current source and constant-voltage regulator with an internal 3.5A switch. The device’s internal PWM dimming generator makes it ideal for driving high current LEDs, and it also has features suitable for charging batteries and supercapacitors. The LT3955’s 4.5 V to 60 V input voltage range suits a wide variety of applications, including automotive, industrial and architectural lighting. The LT3955 uses an internal 3.5 A, 80 V N-channel MOSFET and can drive up to twelve 300 mA white LEDs from a nominal 12 V input, delivering in excess of 20 watts. The device incorporates a high-side current sense, enabling use in boost mode, buck mode, buck-boost mode or SEPIC topologies. The LT3955 can deliver efficiencies of more than 94% in the boost topology, eliminating the need for external heat sinking. A frequency adjust pin permits the user to program the frequency between 100 kHz and 1 MHz, optimizing efficiency while minimizing external component size and cost. Combined with a 5 mm x 6 mm QFN package, the LT3955 offers a compact high power LED Driver solution. The LT3955 has an internal PWM generator that delivers dimming ratios as high as 25:1 or it can utilize an external PWM signal, delivering dimming ratios of up to 3,000:1.

Linear Technology
www.linear.com

Self-powered DC panel mount voltmeter suits battery monitoring

Murata’s DMR20-10-DCM “nanoMeter” is a self-powered auto-ranging DC voltmeter designed for mounting in an industry-standard “oiltight” 30 and 30.5mm round panel cutout. Occupying minimal space, the round voltmeter has a 7.6mm four-digit LED display and is self-powered. Connection to the + 6 to + 75 VDC supply to be monitored is all that is required for full operation. No additional components or separate Power Supply is required for the DMR20, making it extremely easy to add into virtually any equipment using a DC supply or batteries. A user-configurable jumper provides voltage display to a fixed 0.1 V resolution (input + 6 to + 75 VDC) or to a 0.01 V resolution when the input is below + 51 VDC. With its low power consumption, typically less than 7mA, the DMR20 voltmeter is ideal for use in a broad range of battery-powered applications, battery chargers and renewable energy equipment. The voltmeter is packaged in a rugged plastic housing that has been designed to provide protection to IP67 / NEMA 6 specifications for water ingress. It is supplied with an EPDM rubber gasket and plastic hex nut ready to mount in the industry standard panel cutout. The voltmeter is protected against reverse polarity to a maximum of 100 VDC. A self-resetting internal fuse also provides long-term reliability and protection. The DMR20 can operate from – 25 to + 60°C.

Murata
www.murata.eu
**Quad-core PXI embedded controller comes with dual BIOS backup**

The PXI-3980 is Adlink’s first quad-core PXI embedded controller featuring the high-performance Intel Core i7-2715QE 2.1 GHz processor, with up to 16 GB of 1333 MHz DDR3 memory, for seamless execution in multitasking environments and reduced test times. The PXI-3980 features dual BIOS backup, conserving maintenance costs, multiple interfaces for connecting and controlling a wide variety of standalone instruments, user-friendly access design for easy maintenance, and support for hybrid PXI-based testing system control. The PXI-3980’s innovative structure delivers high availability in reliable testing systems. In the event of a main BIOS crash, the secondary BIOS can boot the system and recover the main BIOS, reducing maintenance costs and efforts. Easy maintenance makes battery, storage device, and SODIMM modules swap-out easier than ever. In addition, solid metal case elements protect electrical components and enhance electromagnetic compatibility. Multiple Interface choices are available for connecting and controlling a wide variety of standalone instruments, including two display ports supports for VGA + DVI, dual GbE ports, GBlP, and trigger I/O for advanced PXI trigger functions. The PXI-3980 also includes four USB 2.0 ports and dual hi-speed USB 3.0 ports for connection to storage, easily accessing data from system controllers with limited built-in data storage size, and securing data with no storage damage issues.

**Adlink Technology**

[www.adlinktech.com](http://www.adlinktech.com)

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**WiFi-enabled thermocouple data logging sensor connects to the cloud**

Corintech has launched the EL-WiFi-TC, a battery-powered WiFi-enabled thermocouple data logging sensor that measures the temperature of the environment in which the probe is situated and then transmits data via WiFi to a PC or the company’s EasyLog Cloud (to be released soon). As with other models within the company’s WiFi EasyLog range, the EL-WiFi-TC works with any existing WiFi network. Users only need to download the free PC software application from [www.corintech.com](http://www.corintech.com/support) to configure the sensor and start temperature monitoring. During configuration, the sensor will search for an existing wireless network whilst physically connected to the PC. It can then be placed anywhere within range of the network. If the sensor temporarily loses connectivity with the network, it will log readings until it is able to communicate again with the PC application or cloud service. Logged data is also retained if the battery goes flat, so all data is secure even in unforeseen circumstances. This system allows the user to remotely view and analyse multiple sensors, immediately graph historic data, reconfigure settings and set alarms. Other product features include a temperature measurement range of -270°C to +1300°C, maximum and minimum readings, high and low alarms, rechargeable internal lithium battery and an audit function. It is supplied with a K type probe.

**Corintech**

[www.corintech.com](http://www.corintech.com)

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**Arduino-based development kits for M2M apps include GSM chip and M2M SIM card**

Deutsche Telekom is officially launching its M2M development kits for programmers looking to develop cloud-based machine-to-machine applications. The development kits consist of an Arduino or a Cinterion board with a GSM chip, a SIM card, and access to the M2M Developer Platform. The launch will coincide with the relaunch of the M2M Developer Community, a portal for developing M2M products, solutions, and services. The portal also offers a procedural model illustrating steps during the development of M2M applications – from initial idea, requirements analysis and design to marketing. The M2M DevStarter developer kit bundles all the tools required to get started with machine-to-machine communication. It comes with either an Arduino board or the Cinterion EG55 kit that is designed for developing prototypes in industrial scenarios. Developers who already have the hardware required can order the M2M DevFlex kit. All sets include a SIM card complete with a six-month M2M data tariff and private access to the cloud-based M2M Developer Platform. The platform is supplied by Deutsche Telekom in cooperation with cloud specialist Cumulocity GmbH. Since December 2012, M2M DevFree access has provided a taster of what lies ahead. On a public and shared level, programmers can test the M2M Developer platform free of charge, integrating up to ten devices.

**Deutsche Telekom**

[http://m2m.telekom.com](http://m2m.telekom.com)

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**3U VPX graphics card uses AMD’s 480-core Embedded Radeon GPU**

Kontron has launched a 3U VPX graphics card with AMD Embedded Radeon E6760 GPU, designed to meet the latest demands in avionics and military technology. With its 480 computing cores, the OpenVPX-compliant VX3327 delivers a parallel data processing performance of up to 576 GFLOPs. Equipped with this processing power, board is optimized for compute-intensive General Purpose Graphics Processing Unit (GPGPU) applications deployed in avionics and military technology which require superior situational awareness. Size, Weight, Power and Cooling (SWAP-C) critical applications benefit from the board’s light weight construction, along with minimal power consumption of just 35 watts, plus conduction cooling - withstand extreme temperatures of -40°C to +85°C. Additionally, the board supports real-time graphic data transmission of up to three independently controlled displays, so that users can extend their field of vision across three high-performance screens. For the new VPX graphics card, application areas are to be found predominantly in the field of High Performance Embedded Computing (HPEC). The VPX graphics card is available either in air-cooled (0°C to +55°C) one inch (SHP) or in conduction-cooled (-40°C to +85°C) 0.8 inch (4HP) variants. It supports the operating systems Linux, Windows and VxWorks.

**Kontron**

[www.kontron.com](http://www.kontron.com)
12.7mm diameter slotless brushless DC motor delivers up to 0.0064Nm

The BI-05 Series slotless brushless DC motor was designed by Pittman Motors for maximum precision and performance in a package size perfectly suited for precision equipment such as surgical and dental tools. The BI-05 was developed with stringent design criteria as the focal point. Its slotless motor design eliminates the magnetic cogging typically found in conventionally wound “slotted” brushless DC motors. The stator teeth are completely eliminated by forming and encapsulating the entire stator winding along the inside surface of the back iron. The result is zero detent torque, low inductance and extremely fast response rates. The BI-05 motor body has a 12.7mm diameter and is capable of no-load speeds of up to 60,000 RPM. The miniature motor is rated for a continuous output torque rating of up to 0.0064Nm. The overall motor construction is a combination of 17-, 300, and 400 series stainless steels, the 4-pole rotor is built using high-energy neodymium magnets, and an internal circuit board supports hall sensor feedback spaced at 120 electrical degrees. Other standard features include shielded ball bearings and a tight rotor balancing spec for smooth and quiet operation at high speeds. An autoclavable version of the BI-05 also is available.

Pittman Motors
www.Pittman-Motors.com

3.5x3.55mm SMT side actuated switch takes up to 100,000 cycles

The new SMT side actuated switch series developed by C&K components increases operating life while reducing the footprint. The PTS 840 Series switch is available with front PIP leads that deliver strong shear resistance and higher reliability than other technologies. Combining small size, an extended life span of up to 100,000 cycles, and an optional ESD pin, the robust PTS 840 Series switch is suitable for inclusion in a variety of systems where PCB space is limited, including nomad devices, remote controls, personal health diagnostic systems, and consumer electronics applications. The SMT side actuated switch measures a slim 3.5x3.55mm with a travel path of 0.2mm + 0.2mm / -0.1mm. The momentary action of PTS 840 Series switch with J-, G-, and front PIP-type terminals can withstand contact resistances of under 500ohms and insulation resistances of over 100ohms. Through the use of two-shot moulding, paint and laser etch, pad printing, and plating processes, the switches are designed to stand out. The PTS 840 Series switches exhibit a bounce time of less than 10ms and an operating temperature of -40°C to 85°C.

C&K Components
www.ck-components.com

NFC transponder hardware simplifies Bluetooth and Wi-Fi pairing

Texas Instruments’ Dynamic NFC Transponder RF430CL330H hardware enables uncomplicated and inexpensive wireless set up. The low cost kit brings a secure, simplified pairing process for Bluetooth and Wi-Fi connections to products, such as printers, speakers, headsets, and remote controls, as well as computer peripherals. Designed specifically for NFC connection handover and service Interface functions, the kit includes host diagnostics and software upgrades. The company also announced its NFCLink software firmware library, developed in partnership with Stollman E+V GmbH and Kronenger GmbH to streamlining NFC development across TI's entire embedded processing portfolio. The Dynamic NFC Transponder RF430CL330H combines a wireless NFC Interface and wired SPI/I2C Interface to connect the device to a host (classified as an NFC tag type 4 device). The data content is then shifted dynamically from the host into the RF430CL330H’s SRAM and can then be transferred over the NFC interface. The transponder supports data rates up to 848 KBs per second for RF data transfer (over-the-air firmware updates). It incorporates an ISO 14443B-compliant RF interface, allowing wireless access of NDEF messages. The host wakeup capability in an RF field maximizes battery life.

Texas Instruments
www.ti.com

Quad-core HSPA+ processor with 5G WiFi, NFC, GPS and indoor positioning

Broadcom Corporation has announced a quad-core HSPA+ processor designed for high-performance, entry-level smartphones. The BCM23550 is the company’s latest smartphone platform optimized for the Android 4.2 Jelly Bean operating system (OS). According to research firm International Data Corporation (IDC), the first quarter of 2013 marked the first time that smartphones comprised more than half of all phones shipped globally. This growth is driven by mass market consumers who demand affordable devices that deliver increased functionality and a level of performance that was previously available only in higher-end superphones. The BCM23550, and its turnkey design, are powered by a quad-core processor running at 1.2 GHz, VideoCore multimedia and an integrated HSPA+ cellular baseband that provides enhanced, power-efficient features for entry-level smartphones. The BCM23550 supports “dual HD,” allowing users to simultaneously share high-definition content from a small handheld screen to a larger, Miracast-enabled display. It includes leading VideoCore technology for fluid, responsive graphics and incorporates Power Management techniques to optimize battery life and reduce power consumption without compromising the user experience. The platform provides an integrated Image Signal Processor (ISP) that supports up to 12-megapixel Sensors with advanced imaging capabilities such as blink and smile detection, face tracking, red eye reduction, fast shot to shot (burst capture), zero shutter lag, and best picture selection.

Broadcom Corporation
www.broadcom.com
Industrial 3D-sensor supports shape scanning and 3D data records

The EyeVision image processing software by EVT now also supports the new 3D-sensor EyeScan VR 3D. The sensor, based on digital stripe light projection, that supplies ready-calculated 3D data records for industrial image processing, is also equipped with the complete command set of the EyeVision software and the newly developed 3D commands. Stripe projection, image recording and generation of the point cloud are performed in an integrated manner based on an intelligent camera. The projector from Texas Instruments and the camera are synchronized with a frequency of 60 Hz. The EyeScan VR 3D outputs the recorded 3D data directly as a point cloud or a grayscale-coded range map to the evaluation computer and can be integrated in industrial installations via the Industrial Ethernet interface. Commands applications such as Bin-Picking, 3D-Matching and robot guidance can be programmed easily. The EyeScan VR 3D features a robust metal housing with IP65 protection, screw-type standard industrial connectors, a 24V connection, an Ethernet Interface as well as hardware and software triggers.

Eye Vision Technology
www.evt-web.com

High efficiency power supplies reduce parts count by 80% in automotive applications

Rohm has announced the development of compact, high efficiency Power Supplies designed to drive DDR memory, microcontrollers, and other components in car applications. The BD905xx series integrates a phase compensation circuit and feedback resistor, reducing the number of external parts considerably compared with conventional Power Supply ICs. This simplifies design load and contributes to end-product miniaturization. These Power Supplies use synchronous rectification for high efficiency operation, in combination with Light Load Mode, ensuring superior performance with low current consumption under all load conditions. The chips come in a HTSOP-J8 package, reducing volume by approximately 80% compared with conventional products, claims the manufacturer. Loss is a 10th the level of conventional LDO regulators, resulting in minimal heat generation. This simplifies thermal countermeasures, making it suitable for Microcontrollers and DDR memory used in today’s vehicles that require greater current consumption. Synchronous rectification, coupled with Light Load Mode, results in over 90% efficiency under all load conditions for minimal current consumption. Rohm offers models in different output voltages and currents designed for various automotive systems (1.2V for Microcontroller cores, 1.5V and 1.8V for DDR memory).

ROHM Semiconductor
www.rohm.com/eu

Data acquisition tool for Linux supports digitizer, waveform generator and digital I/O cards

The sixth generation of the SBench 6 Data Acquisition software from Strategic Test is available for both Windows or Linux users. SBench continues to support all of the companies PCI Express, PCI, PXI and CompactPCI digitizer, waveform generator and High-Speed digital I/O cards, some 300 variants in total. The Base version of SBench 6 is supplied at no-cost with each UltraFast card. In addition, a fully functional demo version of the Professional Version with a limited run time is also included. The software is also able to run simulated demo cards to allow full software test even without hardware. For applications that require more features, the SBench 6 Professional version is available for 1190 Euro. Key features of the Professional version include fast Data Acquisition supporting RAID disk arrays, with the capability to acquire and handle GBytes of data. The tool can display analog data, digital data and frequency spectrum. It has integrated analysis functions, an import and export filter, enhanced cursor functions, state-of-the-art drag-and-drop technology and a thread-based program structure. The software is able to measure in Oscilloscope mode as well as long time transient recording mode (streaming mode). A special feature of SBench 6 is the segmented view that allows display of segment based signals together with signals of a second timebase (ABA mode) as well as highly precise timestamps. Besides this SBench 6 data can be exported into ASCII, Wave and MATLAB.

Strategic Test Corporation
www.strategic-test.com

Automotive hub controller ICs now in 7x7x1.0mm 48-pin QFN package

Seiko Epson has begun shipping a new addition to its S2R72A4 series USB hub controller ICs for automotive applications. The series, which is engineered to operate in a temperature range from -40 to 105°C, now includes a 48-pin QFN package measuring only 7x7x1.0mm. The convenience of USB ports is making them a popular choice for automotive equipment such as car navigation systems. Epson’s USB hub controller for automotive applications meet the rigorous quality required by the automotive industry and support stable communications even with long USB cables. The chip has one upstream port and four downstream ports (2 High-Speed ports and 2 full-speed ports). The upstream port is locked in USB full-speed mode and can be used as a USB full-speed hub (USB High-Speed non-supported hub). It can also be locked into USB full-speed even if the destination host supports USB high-speed, which is effective in improving EMI/EMC performance and reducing power consumption. The device operates from LVDD: 1.8 V (internal) HVDD: 3.3 V (USB unit).

Epson Europe Electronics
www.epson-europe.de

www.electronics-eetimes.com  Electronic Engineering Times Europe  July/August 2013 45
ARM Cortex M3-based MCU combines 258 kB of SRAM and 1 MByte of ROM

Toshiba Electronics Europe’s TMPM36BF10FG is a new ARM Cortex M3-based Microcontroller that combines large capacity memory with a range of serial interfaces, integrating measurement and communication systems into a single chip. The TMPM36BF10FG comes equipped with 258 kByte of SRAM and 1 MByte of ROM and is well suited for controlling complex systems that involve large software and data sets. Featuring an optimised circuit design, the TX03 series Microcontroller consumes just two thirds of the power of equivalent products, claims the manufacturer. The Microcontroller is pin-compatible with TMPM36BFYFG, which will have a lower memory capacity and is scheduled to start mass production in November 2013.

Toshiba Electronics Europe
www.toshiba-components.com

ClearSource LED emitters enable precision sensing and detection

Optoelectronics technology company OMC has introduced a range of solid-state emitters that use a new die bonding technique to connect the LED chip electronically to the leadframe, eliminating ‘dark spots’ and improving beam precision. Standard LED optical Sensors use a top-mounting wire bond to connect the LED chip to the anode or cathode. The bond wire obstructs the light output, giving rise to dark spots and patches in the beam which makes precise sensing and detection more difficult. In OMC’s new ClearSource series, the wire is bonded to the side of the chip, leaving the output beam unobstructed. This produces a defined light beam which enables high-accuracy sensing and detection. For even greater precision measurements that require near-parallel light emission, lenses can be incorporated. Additionally, this die-bond configuration reduces capacitive effects within the diode, enhancing switching speed and reliability. According to OMC, ClearSource emitters also benefit from LED technology’s inherent high reliability and long lifetime. The devices have a low sensitivity to ESD, and are suitable for a wide range of applications including encoders, Linear positioning, line and edge sensing, medical equipment, fibre optic systems, machine vision, optical switching, distance and range finding. Devices are available with standard apertures for 650nm and 850nm LEDs with ball-type narrow beam, flat, dome, or drip encapsulation lensing options.

OMC
www.omc-uk.com

Win one of three FiND-iT kits with RFID label tags

Jointly released by the RFID Journal, Microelectronics Technology (MTI) and Enso Detego, the FiND-iT is a PC and Android smartphone or tablet solution that enables users to associate passive ultrahigh-frequency (UHF) radio frequency identification tags with items, as well as create inventory lists and find those objects using an Android smartphone or tablet. This month, Enso Detego gives away three FiND-iT kits for EETimes Europe readers to win, including one MTI RFID ME USB dongle reader, one MTI MINI ME RFID reader for Android hosts, a USB 18-inch extension cable, a USB On-the-Go (OTG) Adapter cable, and 50 pre-encoded and serialized EPC Gen 2 RFID label tags. When the UHF RFID tag is presented to the PC running the FiND-iT software and equipped with MTI’s USB dongle reader, the user can enter information about that object, including its name and location, along with other attributes created by that individual. The Mini Me RFID reader can be attached to any device capable of supporting Android hosts.

Check the reader offer online at
www.electronics-eetimes.com

Bright LED matrix with on-board processor connects to the Raspberry Pi

Internet of Things (IoT) manufacturer Ciseco has released the ‘Pi-Lite’ LED display for the Raspberry Pi. The bright LED matrix has an on-board processor, allowing Raspberry Pi users to display messages and graphics by sending simple commands and text strings to the serial port. The ‘Pi-Lite’ display unit is a pre-built plug & play module, but it can also operate in stand-alone mode, and when combined with one of Ciseco’s radio modules can even form a wireless display unit. The ‘Pi-Lite’ idea comes from the very popular Arduino Lots of LEDs shield by Jimmy Rodgers and brings these capabilities to the Raspberry Pi user. The board features a 9x14 (126) red LED matrix (a white version will be available soon), an on-board Arduino ATMega 328 processor allowing each pixel to be individually addressed, and an on-board controller that can be upgraded or reprogrammed using the standard OptiBoot serial bootloader. The kit comes with Ciseco firmware that will scroll text, display bar graphs, VU meter, and address individual pixels.

Ciseco
www.ciseco.co.uk
All-metal front pushbutton range offers IK10 shock protection and IP67 sealing

EAO has improved the Series 82 pushbutton range with a set of design upgrades to give it the edge over other metal pushbuttons. Series 82 has been re-engineered from the inside out for extra strength, versatility and style. Featuring an all-metal front, IK10 shock protection and IP67 sealing, it is now one of the highest specified pushbuttons on the market. Even extreme temperature fluctuations from -30 to +70°C and humidity up 85% will not affect operation. Control panel designer can now get the look and feel they desire through the wide choice of sizes, lens profiles, illumination styles and finishes including 16, 19 and 22.5mm diameter mounting-hole sizes, with dot or ring illumination, flat, raised or convex lens shapes and various finishes including stainless steel SUS 304 or chromed brass, gold coloured or aluminium anodised. Series 82 is suitable for ticket and vending machines, information terminals, access controls and door entry systems. All component materials adhere to RoHS and UL.

KCB Solutions, an ITAR compliant and AS9100 certified micro-wave design and manufacturing center, has announced a suite of SPST through SP6T switches designed to meet high power-handling requirements from 50 to 200 W. These switches are available in QFN-style packages and thermally conductive flange-mount packages. As an added feature, they are shipped to order in factory-configured ports. As an added feature, they are shipped to order in factory-configured ports. Designed and manufactured with PIN diode technology, they have 100 percent RF tested (small signal), have robust carrier construction, and are manufactured with thick deposition thin film traces. For power levels up to 50 W, KCB offers these high power switches in surface mount packages. They offer low-loss performance from DC to 6 GHz and robust construction. To address the need for switches that can handle powers in excess of 50 W, KCB has developed a flanged-based package. By utilizing an AIN carrier with a CuW sub-mount, the construction of these products offers superior heat spreading which allows for CW incident power levels up to 200 W. This, coupled with larger minimum breakdown voltages, provides the designer with a switch that is ideally suited for higher powered radios, Radar and counter IED systems. These models are available in configurations up to SP3T. KCB offers several off-the-shelf configurations as well as dozens of possible configurations that can be quickly realized using off-the-shelf components. In addition, the designer can choose from a menu of diodes that provide optimal linearity for the application.

KCB Solutions
www.kcbsolutions.com

Isolated USB analog output modules support up to eight continuous waveforms

Data Translation’s enhanced performance versions of its DT9853 and DT9854 USB analog output modules come with four or eight outputs with 16-bit resolution and can now also provide continuous analog waveform streaming at up to 8 kHz. ±300 V galvanic isolation ensures safe operation, high signal integrity and excellent noise performance even in harsh industrial environments. All modules provide voltage outputs (±10 V, 0-10 V). The M versions have additional 0-20 mA current outputs supporting an external excitation voltage supply of 8-36 V. Key features include eight digital inputs, eight digital outputs and a 32-bit counter/timer. The interrupt on change function can be used on up to seven digital inputs to monitor and control critical signals. The analog output modules offer plug-and-play USB 2.0 connectivity to PC. They run entirely on USB power so that no external Power Supply is needed. The rugged enclosure as well as screw terminals for signal connections support industrial testing, control loop and process control applications. A comprehensive software package is included with the modules. In addition to Windows-compatible 32/64 bit drivers for Windows SDK or .NET, the package also provides interfaces for LabVIEW and MATLAB.

Data Translation
www.datatranslation.eu

Switches cover DC to 6 GHz for applications up to 50 through to 200 W

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KCB Solutions
www.kcbsolutions.com

TCXOs comes with stabilities to ±1 ppm in custom frequencies up to 250MHz

Fox Electronics now offers its XpressO TCXO with tighter stabilities in custom frequencies up to 250MHz. Available with ±1.5 ppm from -40 to +85°C as well as down to ±1 ppm from 0°C to +70°C, the XpressO-TC HCMOS TCXO oscillators can be delivered in ten working days or less. These new TCXOs are an expansion to Fox's FXTC-HE73 series that meets the humidity, shock and vibration requirements of MIL-STD-202. They are suitable for applications requiring very tight stability over temperature and low jitter, including medical monitoring and measurements, telecommunication and networking as well as military communications. Surpassing the typical 50 to 60MHz frequency range of traditional TCXOs, the new XpressO-TC oscillators offer a significant performance advantage, since custom frequencies can be specified up to 250 MHz. Fox’s proprietary ASIC technology, with a 3rd order Delta Sigma Modulator (DSM), enables XpressO oscillators to significantly reduce noise to levels comparable with traditional bulk quartz and SAW oscillators. This ASIC family enables the selection of output type, input voltages and temperature performance within the oscillator.

Fox Electronics
www.foxonline.com
Versatile RFID reader is optimised for a read range up to 2m

The Ha-VIS RF-R200 is the latest RFID reader in Harting’s range of auto-ID solutions, it is a mid-range unit optimised for read ranges up to 2m. The RF-R200 reader is available in a number of different versions to suit the requirements of diverse applications. These include a model with an RJ45 Interface and PoE (Power over Ethernet) capability, a unit with a USB Interface designed for office use, and a basic PCB module without housing for integration into machines or other products. Key features of the RF-R200 reader include 500 mW of transmitter power, support for automatic transmission of the acquired transponder information to a computer, and support for an external antenna as well as the internal antenna with a read range up to approximately 20 cm. The unit is sealed to IP 30 requirements, and occupies a minimum footprint when installed on a “top hat” rail in a switch cabinet.

Harting
www.harting.com
AUO 22” 1/3 cut TFT for every application

Besides the common 4:3 format TFTs, Data Modul now offers AUO’s full product line up for wide format 16:10 displays. A new “stretch-format” also makes it possible to provide panels into new applications where no suitable panel was available before.

New kit turns Raspberry Pi boards into low-cost home media centres

Raspberry Pi owners can now quickly and easily turn their Pi into a low-cost media centre for their home or office, with a new XBMC bundle from element14. One of a strong pipeline of Raspberry Pi solutions to be launched this year, the XBMC bundle is available through Farnell element14 in Europe. Containing all the additional hardware and software necessary to start using the device, the starter kit will allow users to stream content from devices on their home network through their Raspberry Pi, turning the screen or their TV into a media centre. The XBMC bundle includes an SD card pre-loaded with Raspbmc software, an open source Linux distribution created by Sam Nazarko that brings Xbox Media Center (XBMC) to the Raspberry Pi.

“AuPc” Electronic Industry Company (AUO) GmbH has started to design and build its own line of LED modules. Its first product is a low-cost module with single-chip LEDs. The E-104-MC3/6xx-F5 is available in two versions, with 3 and 6W, respectively. The new modules are manufactured in collaboration with manufacturing design and services company Turck Duotec GmbH. They can replace the 3W and 6E variants of Citizen’s LED CL-L104 since they have the same form factor and size. The E-104-MC3/6xx-F5 is available five color temperatures ranging from 2700K to 5000K. As an example, the 3W 3000K version is supplied with a DC constant current of 350mW provides 104lm/w and 328lm.

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Prototyping to production”, the new Digi-Key trademark

Digi-Key has received registered trademarks for the phrases, “Prototype to Production®” and “From Prototype to Production®” in line with the company’s unique distribution model in the electronic component industry. “Digi-Key’s leading-edge business model is unique in its ability and strength to support product from the design phase, through new product introduction runs and high-mix/low volume production,” said Digi-Key president, Mark Larson. The company’s “prototype to production” capabilities allow engineers to engage long-term with a go-to partner and maintain their engagement through production.

Low-cost module with single-chip LEDs

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Endrich Bauelemente Vertriebs GmbH

www.endrich.com

Data Modul

www.data-modul.com

Arrow Electronics

www.arrowvaluerecover.com

Rutronik

www.rutronik.com

Element14

www.element14.com/raspberrypi

Digi-Key

www.digikey.com

www.element14.com/raspberrypi
LAST WORD

Wearable computing: let’s get it on

By Rick Merritt

I AM CONVINCED ULTRA-MOBILE wearable computers will be the next big thing, but it could take a decade before the iPhone of this product class arrives. With Project Glass, Google is intentionally trying to leap ahead, creating a very public prototyping process that is fascinating but by no means guarantees success.

Gordon Bell, an industry veteran investigating the field at Microsoft Research, helped me crystalize my belief in wearables when I chatted with him informally at a recent event celebrating the 40th anniversary of Ethernet.

He told me facial recognition and medical sensing are two killer apps for these products. Bell wore a mobile camera everywhere he went as part of his research program. “What I concluded is that [wearable computers] are a memory assistant,” and facial recognition plays a key role in that job, he told a group of us over lunch.

Ironically, the Glass project manager at Google recently said the company currently has no plans to use facial recognition. I suspect that statement was motivated at least in part by privacy concerns and in part by the still nascent state of the technology.

I believe tomorrow’s wearables will need to tap into highly accurate facial recognition services and find ways to overcome privacy concerns about them.

There’s hard technical work ahead making facial recognition of unconstrained populations really accurate—especially when the data is gathered in the normal course of life using consumer-grade cameras. Making the challenge even tougher, facial recognition systems must handle data sent over mainstream wireless networks, and these systems must respond in time to be useful to the average users as they casually encounter other people.

I can’t even begin to untangle the marketing and policy issues around facial recognition. I know they are significant. Like Bell, I believe the app is killer for the product category. Wearables could also revolutionize healthcare. Researchers at Belgium’s imec and elsewhere have been working on body area networks for many years, making stepwise advances. Today, Bell wears a Fitbit heart rate monitor. He also has invested in multiple startups specializing in wearable health devices, including Bobo Analytics, which makes a heart sensor worn like a wristwatch.

“I feel strongly you have to get healthcare out of the hands of people like cardiologists,” he told me.

He and others see a future where people are continuously monitored. Cloud services analyze and track the data, reporting and hopefully anticipating problems.

Here again, there are technical and market/policy issues. For example, so-called dry sensors casually worn in clothes and accessories have to get much better in collecting accurate data in the midst of the noise in and around the body. And I don’t even want to open the Pandora’s box of policy issues around liability and reimbursement. They make the debate around Obamacare sound like chamber music. It’s fascinating to watch the growing number of people involved with Google tinker more or less in the public eye with a prototype of the next big thing. But let’s get some perspective here—they are far from the first pioneers in this field.

I covered DARPA programs on wearables more than a decade ago. Many small, less visible companies are doing all sorts of wearables today, mainly for fitness enthusiasts—a sector that doesn’t have to tackle the healthcare policy issues.

Google is clearly getting mindshare with Project Glass, but that doesn’t necessarily translate into marketshare. The hurdles ahead are still huge, including the limits on battery power given what the average person wants to carry. Some day, Apple or some other company could just surprise us with an iWatch or iBelt or iShirt—or, yes, iGlasses—designed to capture the sort of thing the market wants but hasn’t been able to articulate. I see great potential here for a set of wearable products that work in concert.

For many years researchers at Philips and elsewhere (especially in Europe) have been working on conductive yarns. Their goal has been to sew wearable sensors directly into clothes. This is really cool stuff, but it likely represents a generation of wearables well beyond the first crop of watches, glasses, and belts. When we get to the stage of woven electronic computers, the technology and fashion worlds will collide in a way that makes smartphone cases look like Hello Kitty dolls.

I’m guessing really useful ultra-mobile wearables won’t come for years, given the many challenges ahead. What fun it will be watching this next big thing emerge.
Haswell - the 4th Generation Intel® Core™ processor platform

This white paper discusses the implementation of Intel’s new generation Core Processor Platform in its series of Embedded boards available in most popular form factors and bus technologies. Benefits include lower power, higher speed, much better graphics, 6Gb/s SATA ports, as well as I/O flexibility allowing to set ports to USB 2.0 or 3.0.


Lighting applications – lighting the way with LEDs

LEDs are being rolled out as replacements for incandescent lighting throughout the world. The Chinese government has a very strong commitment to LEDs, especially in street lighting. In the U.S. and Canada, the LED market share of lighting is estimated at around 7 percent. LEDs offer many advantages that are compounded by the length of time they are used. Greg Quirk from Mouser Electronics gives an overview of this process in the different countries and introduces the role of OLEDs.


Replacing the candle in the candelabra

Two compact, efficient bulb-replacement design ideas. By moving to a buck boost topology, PI is able to achieve a combination of performance that has not been possible up to now. Previously if a design was required to deliver very high efficiency, a high output voltage was required. However, this concession to efficiency resulted in unacceptably low power factor and total harmonic distortion that made such solutions unusable for worldwide lighting applications.


High voltage surge stoppers ensure reliable operation during power surges

In automotive, industrial and avionic applications, high voltage power supply spikes with durations ranging from a few microseconds to hundreds of milliseconds are commonly encountered. The electronics within these systems must not only survive transient voltage spikes, but in many cases also operate reliably throughout the event. In systems where power is distributed over long wires, severe transients are generated by load steps (abrupt changes in load current).


16-Bit, 100 kSPS low power successive approximation ADC system

This application note describes a 16-bit, 100 kSPS successive approximation analog-to-digital converter (ADC) system that has a drive amplifier that is optimized for a low system power dissipation of 7.35 mW for input signals up to 1 kHz and sampling rates of 100 kSPS. This approach is highly useful in portable battery powered or multichannel applications, or where power dissipation is critical.


ZVS buck regulator removes barriers To increased power throughput

The need for higher power density in today’s electronic systems combined with higher overall efficiency has driven many changes in the Non-isolated Point-of-Load Regulator (niPOL). While the solutions developed work well over a narrow voltage range, the efficiency and throughput power tend to drop dramatically when they are subjected to a wide input range. This paper looks at a new ZVS buck regulator topology.


Supporting multicore SoCs in critical embedded systems for avionics, defense and transport

Avionics, Defense and Transport, like all high-end processing application areas, are looking for ways to increase performance and at the same time reduce the existing form-factor and power budgets. If COTS multicore SoCs (System-on-Chip) stand as the common approach to meet these design goals today, their use in critical embedded systems introduces some new paradigms when considering key goals related to safety and certification.


Leveraging high-volume CMOS manufacturing for MEMS-based frequency control

Over the last five years, microelectromechanical systems (MEMS) solutions have steadily eroded the 100-year-old monopoly held by quartz crystal solutions for frequency control and timing products. MEMS technologies, originally designed around the promise of smaller form factors, have enabled significant additional advantages related to lead time, supply stability, product reliability, device size, and price and performance tradeoffs.
- searches all electronics sites
- displays only electronics results
- is available on your mobile

www.eetsearch.com